40 / 100 Gigabit Ethernet PCS Cores Product Brief

Version 1.3 - February 2010

Introduction

The 40 Gigabit and 100 Gigabit Ethernet Base-R PCS Cores are compliant to the IEEE802.3ba Specification and are designed to be used in conjunction with the MorethanIP 40 / 100 Gigabit MAC Cores to create flexible system solutions for 40 and 100 Gigabit Ethernet LAN applications. The 40/100GBase-R PCS Cores include the 40 / 100 GbE scrambler/descrambler, the 64b/66b encoder/decoder, multi-lane distribution, alignment marker insertion/striping, block synchronization and gearbox as well as clock and rate decoupling elastic buffers.

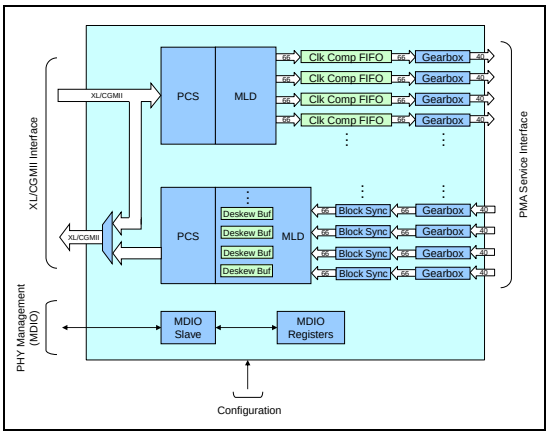
The MLD (Multi-Lane Distribution) module distributes data across 4 or 20 virtual lanes for 40 Gigabit or 100 Gigabit, respectively. This allows all data from a virtual lane to be transmitted over any optical/electrical lane combination and variation. This ensures that the data from a virtual lane is always received with the correct bit order at the Receiver. Periodic alignment markers are added to each virtual lane, which allow the Receive PCS to perform skew compensation, realign the virtual lanes, and reassemble a single 40 Gigabit or 100 Gigabit aggregate stream.

On the application side, the Cores implement either a XLGMII (40 Gigabit Medium Independent Interface) or a CGMII (100 Gigabit Medium Independent Interface), depending on the Core.

On the line side, the 40/100GBase-R PCS Cores implement a flexible SERDES interface supporting 16bit to 40bit wide parallel data per lane.

The Core clock structure is designed to reduce the load on the Serdes clocks to improve routability and to provide rate matching functionality with minimum latency and delay variation.

No PLL with complex division / multiplication ratio is needed, improving jitter performances and optimizing FPGA resources.



40/100GBase-R PCS Cores Block Diagram

40 / 100 Geth PCS Cores Features Overview

- 40GBase-R or 100GBase-R PCS solutions compliant with IEEE802.3ba Specification Draft
- Can be used together with any 40 or 100 Gigabit Ethernet PHY application or in integrated 40 / 100 Gigabit Ethernet controller devices
- Transmit and Receive data-path operating at 261MHz
- 192-bit XLGMII to a 40 Gigabit Ethernet MAC or 384-bit CGMII to a 100 Gigabit Ethernet MAC
- 4 lanes (40 Gigabit) or 10 lanes (100 Gigabit) line interface with flexibility to use 16/20/32/40 bit SERDES interfaces
- Multi-Lane Distribution (MLD) across 4 or 20 Virtual Lanes for 40 Gigabit or 100 Gigabit, respectively
- Periodic Alignment Marker insertion / striping on transmit / receive, respectively
- Implements 40 / 100 Gigabit Ethernet data Scrambler which generates transition rich signals to the application high speed optical link on the Core transmit path, and data De-Scrambler on the Core receive path
- 64b/66b Encoder / Decoder performing 66-bit block synchronization, 64b/66b receive path decoding, 64b/66b transmit path encoding, and 66b/64b transmit path conversion for block overhead bits
- Simple Clock Structure Optimized for Low Latency and Low Delay Variation
- Programmable loopback on the Core XL/CGMII interface available for application test
- Implements Bit Error Rate (BER) monitoring, with high error rate indication, providing constant line quality monitoring
- Can be seamlessly connected to the MorethanIP 40 / 100 Gigabit Ethernet MAC to build single chip 40 / 100 Gigabit Ethernet controller
- Optional serial Management Data Interface (xMDIO). The management interface provides access to the internal registers of the PCS according to the Clause 45 definition of extended MDIO of 802.3ae
- Available for Altera Stratix IV GT FPGAs
- Complete design kit which includes behavioral Ethernet frame generators and checking models, PCS traffic generation model, standard compliance scenario and implementation scripts

40 / 100 Gigabit Ethernet PCS Cores Product Brief

Version 1.3 - February 2010

Implementation Summary

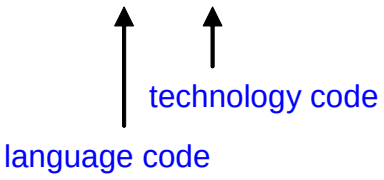
Core Specifics		
Supported Device Family	FPGA: Stratix IV GT / Stratix IV ASIC	
Resources Used		
	40GBase-R PCS	*100GBase-R PCS*
ALUTs	12000	42000
Registers	11000	37000
RAM	32Kbits	34Kbits
Supported Design Tools		
Altera Tool	Quartus II 9.0 or Later	
Synthesis	Quartus II 9.0 or Later Synopsys DC (any)	
Speed Grade		
-C2/C3		

Deliverables

- Verilog / VHDL Synthesizable RTL HDL or encrypted RTL for FPGA implementation
- Behavioral Self Checking Verilog or VHDL testbenches and Verification test cases
- Comprehensive Documentation, Datasheet and User Guide
- Industry-standard Synopsys Design Constraints (SDC) File for Synthesis and Timing Analysis
- Support Directly by MorethanIP Expert Developers

Ordering Code

MTIP-40G_RPCS-lang-tech
MTIP-100G_RPCS-lang-tech



Language Code	***Delivery Language***
VHDL	Synthesizable RTL VHDL Source Code.
VLOG	Synthesizable RTL Verilog Source Code.
BIN	Encrypted RTL for Altera FPGA technology.

Technology Code	***Target Technology***
GEN	Generic synthesizable code for ASIC or FPGA implementations.
ALTR	Synthesizable code optimized for Altera FPGAs.

Contact

MorethanIP GmbH
Muenchner Strasse 199
D-85757 Karlsfeld
Germany
Tel : +49 (0) 8131 333939 0
FAX : +49 (0) 8131 333939 1

E-Mail : info@morethanip.com
Internet : www.morethanip.com