HiGig / HiGig+ / HiGig2 MAC Core with FIFO

Version 2.0 - August 2006

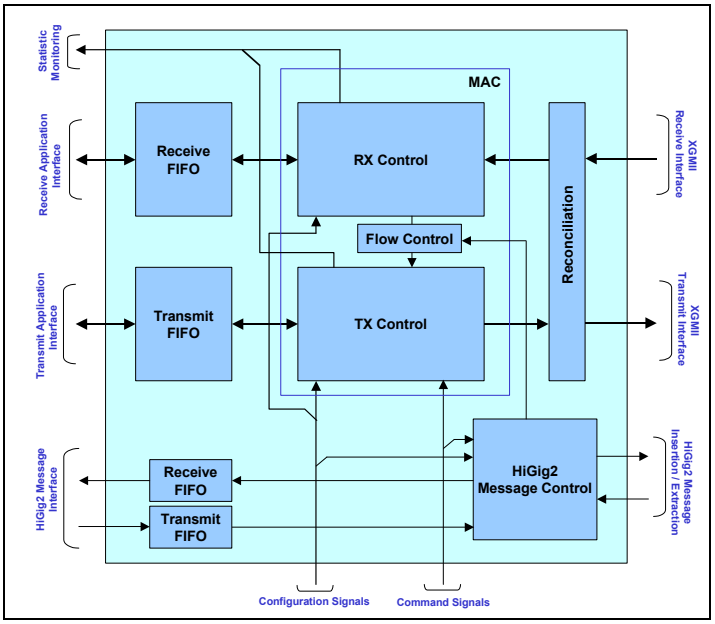
Introduction

The HiGig / HiGig+ and HiGig2 Protocols provide a standard mechanism to interconnect switches to for a single system and is defines to efficiently forward Frames for Unicast, Broadcast, Multicast (Layer 2 and IP) and Control Traffic. The HiGig / HiGig+ Protocol implements HiGig Frames, which are formed by tagging with a 12-Byte HiGig header standard Ethernet Frames, the HiGig2 Protocol implements 16-Byte header.

The 10 Gigabit HiGig / HiGig+ / HiGig2 MAC Core provides a solution to interconnect standard Ethernet devices to Switch HiGig Ports and can be implemented in FPGAs or ASIC devices. The HiGig / HiGig2 MAC Core is compliant with the Broadcom HiGig and HiGig2 protocol definition.

The MAC Core implements, on the Application side, a flexible FIFO interface that is designed to be seamlessly connected to any standard Core (e.g. SPI-4 or POS-PHY L4) compatible with the Altera Atlantic specification. The Core FIFO interface is also designed to allow easy insertion and extraction of HiGig / HiGig2 Header to / from a Switch HiGig / HiGig2 port.

On the Line side, the Core can be configured to implement either a XGMII (10 Gigabit Medium Independent Interface) or a XAUI (10 Gigabit Attachment Unit Interface) when the design is targeted to Stratix II GX FPGAs. Typically, the XGMII interface is selected when the Core is integrated, together with custom logic, in a FPGA or an ASIC solution while the XAUI interface provides a simpler 16-Bit board level interface to connect the HiGig MAC to a Switch HiGig / HiGig+ / Higig2 Port, for example, via a serial Backplane.



HiGig / HiGig+ / HiGig2 MAC Core Block Diagram

MAC Core Features Overview

- Supports the HiGig / HiGig+ and HiGig2 Protocols with dynamic configuration
- Optional XAUI interface implemented with embedded Quad SERDES providing an efficient board level interface to optical modules and loopback
- Lane, data alignment, PHY error and local/remote fault signaling handled by the Core's Reconciliation sub-layer
- CRC-32 checking at full speed using a multi-stage CRC calculation architecture with optional forwarding of the FCS field to the user application
- CRC-32 generation and append on transmit or forwarding of user application provided FCS selectable on a per-frame basis
- Optional MAC address comparison on receive and overwrite on transmit for NIC applications
- HiGig / Higig2 header extraction on Receive and insertion on Transmit to simplify the design of the Client application
- Implements HiGig2 preemptive transmission of HiGig2 messages
- Selectable promiscuous frame receive mode and transparent MAC address forwarding on transmit
- Optional Multicast address filtering with 64-bin hash code lookup table on receive reducing processing load on higher layers
- Ethernet Pause Frame (HiGig / HiGig+ Mode) or HiGig2 Link Level Pause Message (HiGig2 Mode) termination providing fully automated flow control without any user application overhead
- Optional forwarding of received pause frames to the user application
- Automatic Pause Frame generation (HiGig / HiGig+ Mode) or Link Level HiGig2 Pause Messages (HiGig2 Mode) from programmable FIFO congestion thresholds or by dedicated command pin with programmable Quanta
- Programmable frame maximum length providing support for any frame (e.g. Jumbo Frame or any tagged Frame)
- Deficit Idle Counter (DIC) for optimized performance with minimum IPG
- Clock and data rate decoupling with programmable asynchronous FIFOs
- 64-Bit Client application interface compatible with Altera Atlantic SOC (System On-Chip) interface

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Implementation Summary

Altera FPGA Implementation Summary

Target Device Family	Speed Grade	Complexity	Performance
Stratix II	C5	5,170 to 9,220 LEs (1)	190MHz
Stratix II GX	C5	5,120 to 9,170 LEs (1)	190MHz
Cyclone II	C6	6,580 to 11,660 LEs	165MHz

1. The Logic Element count for Stratix II devices is based on the number of adaptive look-up tables (ALUTs) used for the design as reported by the Quartus II software.

Target Device Family	Complexity	Performance
Hardcopy II	28,390 to 52,770 HCells	210Mhz

Deliverables

- Verilog / VHDL Synthesizable RTL HDL or encrypted RTL for FPGA implementation
- Behavioral Verilog or VHDL testbenches and Verification test cases
- Support for FPGA and ASIC design tools

Development Boards

- Standard Stratix II GX FPGA Prototyping / Development Boards
- Comprehensive 10 Gigabit Ethernet PHY Selection

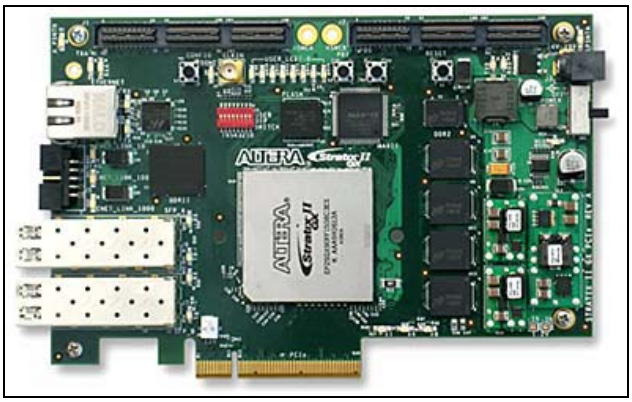

Figure 1: Prototyping / Development Board

Contact

MorethanIP

E-Mail : info@morethanip.com
Internet : www.morethanip.com
Muenchner Strasse 199
D-85757 Karlsfeld
Germany

Tel : +49 (0) 8131 333939 0
FAX : +49 (0) 8131 333939 1