

Introduction

The HiGig / HiGig+ and HiGig2 Protocols provide a standard mechanism to interconnect switches to for a single system and is defines to efficiently forward Frames for Unicast, Broadcast, Multicast (Layer 2 and IP) and Control Traffic. The HiGig / HiGig+ Protocol implements HiGig Frames, which are formed by tagging with a 12-Byte HiGig header standard Ethernet Frames, the HiGig2 Protocol implements 16-Byte header.

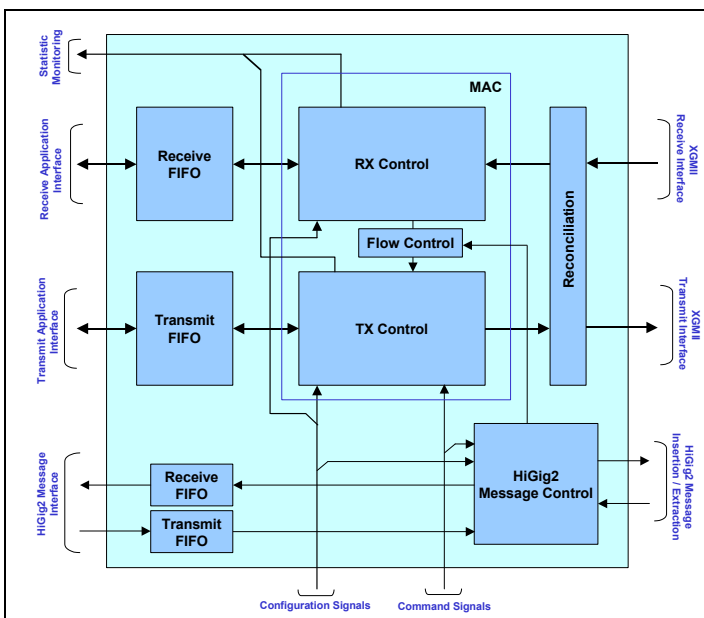
The 10 Gigabit HiGig / HiGig+ / HiGig2 MAC Core provides a solution to interconnect standard Ethernet devices to Switch HiGig Ports and can be implemented in FPGAs or ASIC devices. The HiGig / HiGig2 MAC Core is compliant with the Broadcom HiGig and HiGig2 protocol definition.

The MAC Core implements, on the Application side, a simple and flexible FIFO interface that is designed to be seamlessly connected to any third party Cores (e.g. SPI-4 or POS-PHY L4). The Core FIFO interface is also designed to allow easy insertion and extraction of HiGig / HiGig2 Header to / from a Switch HiGig / HiGig2 port.

On the Line side, the Core can be configured to implement either a XGMII (10 Gigabit Medium Independent Interface) or a XAUI (10 Gigabit Attachment Unit Interface) when the design is targeted to Virtex 5 LXT FPGAs. Typically, the XGMII interface is selected when the Core is integrated, together with custom logic, in a FPGA or an ASIC solution while the XAUI interface provides a simpler 16-Bit board level interface to connect the HiGig MAC to a Switch HiGig / HiGig+ / Higig2 Port, for example, via a serial Backplane.

MAC Core Features Overview

- For Switch Interconnect applications, supports HiGig / HiGig+ and HiGig2 Protocols and SAFC with HiGig and HiGig+
- XAUI interface implemented with embedded Quad SERDES providing an efficient board level interface to optical modules
- Lane, data alignment, PHY error and local/remote fault signaling handled by the Core's Reconciliation sub-layer
- CRC-32 checking at full speed using a multi-stage CRC calculation architecture with optional forwarding of the FCS field to the user application
- CRC-32 generation and append on transmit or forwarding of user application provided FCS selectable on a per-frame basis
- Optional MAC address comparison on receive and overwrite on transmit for NIC applications
- HiGig / Higig2 header extraction on Receive and insertion on Transmit to simplify the design of the Client application
- Implements HiGig2 preemptive transmission of HiGig2 messages
- Selectable promiscuous frame receive mode and transparent MAC address forwarding on transmit
- Ethernet Pause Frame (HiGig / HiGig+ Mode) or HiGig2 Link Level Pause Message (HiGig2 Mode) termination providing fully automated flow control without any user application overhead
- Automatic Pause Frame generation (HiGig / HiGig+ Mode) or Link Level HiGig2 Pause Messages (HiGig2 Mode) from programmable FIFO congestion thresholds or by dedicated command pin with programmable Quanta
- Optional forwarding of received HiGig pause frames to the user application
- Programmable frame maximum length providing support for any frame (e.g. Jumbo Frame or any tagged Frame)
- Deficit Idle Counter (DIC) for optimized performance with minimum IPG
- Clock and data rate decoupling with programmable asynchronous FIFOs
- 64-Bit Client application interface compatible



HiGig / HiGig+ / HiGig2 MAC Core Block Diagram

Implementation Summary

Xilinx FPGA Implementation Summary

Core Specifics		
Supported Device Family	Virtex 5 LXT	
Version	2.0	
Resources Used		
	Min	Max
LUTs	4,100	5,450
FFs	4,900	6,680
Provided with Core		
Documentation	Datasheet, User Guide	
Design File Formats	RTL Verilog, NGC Netlist	
Constraints File	UCF File	
Verification	Verilog Self-Checking Testbench	
Supported Design Tools		
Xilinx Tool	9.1i or Later	
Simulation	Modelsim 5.7 or Later	
Synthesis	XST	
Application Support		
Application	Required Speed Grade	
HiGig	-1	
HiGig+	-2	
HiGig2	-2	

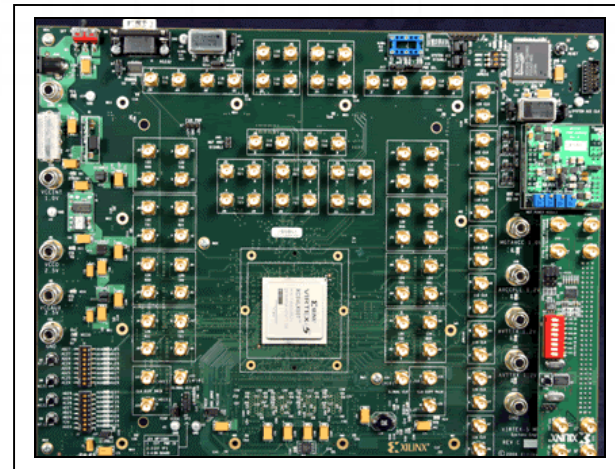


Figure 1: Prototyping / Development Board

Contact

MorethanIP

E-Mail : info@morethanip.com

Internet : www.morethanip.com

Muenchner Strasse 199

D-85757 Karlsfeld

Germany

Tel : +49 (0) 8131 333939 0

FAX : +49 (0) 8131 333939 1

Development Boards

- Standard Xilinx ML 523 Virtex 5 FPGA Prototyping / Development Board