

Introduction

The 10 Gigabit Ethernet MAC Core is designed to comply with the IEEE802.3ae specification and meets the requirements for both WAN / MAN and LAN connectivity. The Version 2 of the Core can be used in either NIC (Network Interface Card) or Ethernet Switching applications. A set of configuration pins is available to dynamically set the Core to terminate and form MAC frames (NIC application) or to pass MAC frames without modification to the User application or to the Ethernet Line (Switching application). When use in NIC or Switching application, the Core provides support for IEEE managed objects, IETF MIB-II and RMON for management applications (e.g. SNMP).

The 10 Gigabit Ethernet MAC Core, on the Application side, a direct Interface that can be connected to a custom user application synchronous to the Ethernet Transmit and Receive clocks.

On the Ethernet Line side, the Core can be configured to implement either a XGMII (10 Gigabit Medium Independent Interface) or a XAUI (10 Gigabit Attachment Unit Interface) when the design is targeted to Altera StratixGX and Stratix-IIGX FPGA.

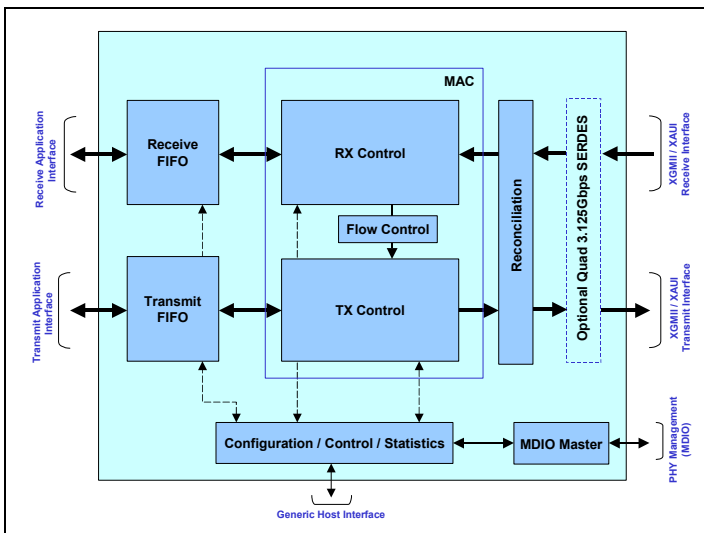
MorethanIP also provides the 10GBase-R and 10GBase-X PCS Cores that can be used, in conjunction with the 10 Gigabit Ethernet MAC, to implements XAUI or XF1 interfaces.

The core is delivered in generic VHDL or Verilog synthesizable HDL code.

The Core is UNH certified and is interoperable with major PHY vendor and systems.

10 Gigabit Ethernet MAC Core Features Overview

- Full MAC layer and Reconciliation sub-layer implementation compliant with IEEE802.3ae specification
- Passed UNH MAC, Flow-Control, Reconciliation and Inter-Operability tests
- Can be dynamically configured for NIC (Network Interface Card) applications or Switching / Bridging applications
- Standard preamble and SFD (Start of Frame delimiter) insertion and deletion with optional insertion of a user specific 8-Byte preamble
- Lane, data alignment, PHY error and local/remote fault signaling handled by the Core's Reconciliation sub-layer
- Optional MAC address comparison on receive and overwrite on transmit for NIC applications with programmable promiscuous mode operation
- Optional Multicast address filtering with 64-bin hash code lookup table on receive reducing processing load on higher layers
- Optional Ethernet Pause Frame (802.3 Annex 31A) termination providing fully automated flow control without any user application overhead
- Optional automatic Pause Frame generation from programmable FIFO congestion thresholds or by dedicated command pin with programmable Quanta
- Programmable frame maximum length providing support for any frame (e.g. Jumbo Frame or any tagged Frame)
- Support for VLAN tagged frames according to IEEE 802.1Q specification in both transmit and receive
- Dynamic inter packet gap (IPG) calculation for WAN applications
- Deficit Idle Counter (DIC) for optimized performance with minimum IPG for LAN applications
- Clock and data rate decoupling with programmable asynchronous FIFOs
- Status word available with each Frame on the User interface providing information such as frame length, VLAN Frame type indication and error information
- Preamble and SFD (Start of Frame delimiter) insertion and deletion
- Optional statistics 32-Bit or 64-Bit counters for IEEE 802.3 basic and mandatory Management Information Database (MIB) package as well as Ethernet MIB (RFC 2665) and Remote Network Monitoring (RFC 2819)



10 Gigabit Ethernet MAC Core Block Diagram

Implementation Summary

Altera FPGA Implementation Summary

Target Device Family	Speed Grade	Complexity	Performance
Stratix III	C4L	4,600 to 8,600 LEs (1)	160MHz
	C4		180MHz
Stratix II	C5	4,150 to 8,100 LEs (1)	190MHz
Stratix II GX	C5	4,200 to 8,150 LEs (1)	190MHz
Cyclone II	C6	6,900 to 11,800 LEs	165MHz

1. The Logic Element count for Stratix II devices is based on the number of adaptive look-up tables (ALUTs) used for the design as reported by the Quartus II software.

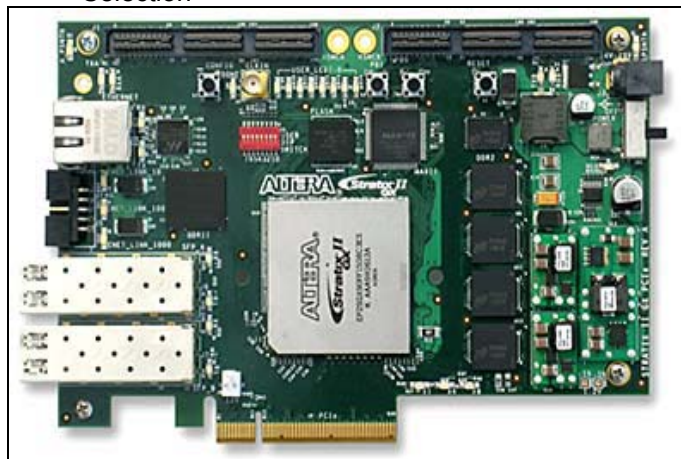
Target Device Family	Complexity	Performance
Hardcopy II	34,700 to 59,000 HCells	210Mhz

Deliverables

- Verilog / VHDL Synthesizable RTL HDL or encrypted RTL for FPGA implementation
- Behavioral Verilog or VHDL testbenches and Verification test cases
- Support for FPGA and ASIC design tools

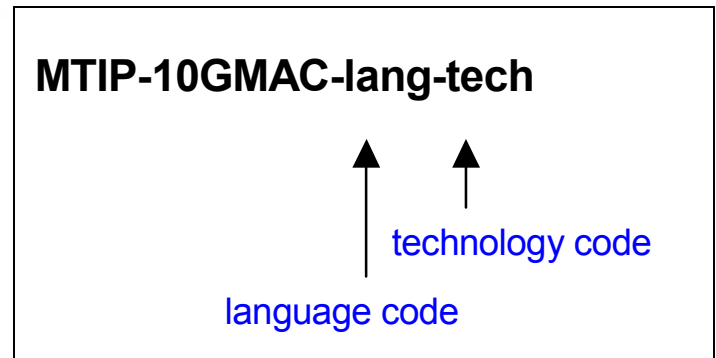
Development Boards

- Standard Stratix II GX FPGA Prototyping / Development Boards
- Comprehensive 10 Gigabit Ethernet PHY Selection



Prototyping / Development Board

Ordering Code



Language Code	Delivery Language
VHDL	Synthesizable RTL VHDL Source Code.
VLOG	Synthesizable RTL Verilog Source Code.
BIN	Encrypted RTL for Altera FPGA technology.

Technology Code	Target Technology
GEN	Generic sythesizable code for ASIC or FPGA implementations
ALTR	Synthesizable code optimized Altera FPGAs.

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