10 Gigabit Ethernet MAC Core Product Brief

Version 3.1 - December 2006

Introduction

The 10 Gigabit Ethernet MAC Core is designed to comply with the IEEE802.3ae specification and meets the requirements for both WAN / MAN and LAN connectivity. The Version 2 of the Core can be used in either NIC (Network Interface Card) or Ethernet Switching applications. A set of configuration pins is available to dynamically set the Core to terminate and form MAC frames (NIC application) or to pass MAC frames without modification to the User application or to the Ethernet Line (Switching application). When use in NIC or Switching application, the Core provides support for IEEE managed objects, IETF MIB-II and RMON for management applications (e.g. SNMP).

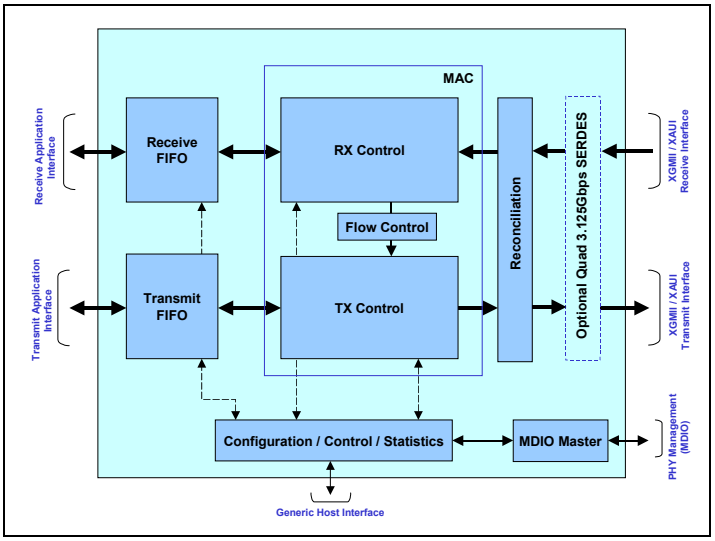
The 10 Gigabit Ethernet MAC Core, on the Application side, a direct Interface that can be connected to a custom user application synchronous to the Ethernet Transmit and Receive clocks.

On the Ethernet Line side, the Core can be configured to implement either a XGMII (10 Gigabit Medium Independent Interface) or a XAUI (10 Gigabit Attachment Unit Interface) when the design is targeted to Xilinx Virtex 5T FPGA.

MorethanIP also provides the 10GBase-R and 10GBase-X PCS Cores that can be used, in conjunction with the 10 Gigabit Ethernet MAC, to implements XAUI or XFI interfaces.

The core is delivered in generic VHDL or Verilog synthesizable HDL code.

The Core is UNH certified and is interoperable with major PHY vendor and systems.



10 Gigabit Ethernet MAC Core Block Diagram

10 Gigabit Ethernet MAC Core Features Overview

- Full MAC layer and Reconciliation sub-layer implementation compliant with IEEE802.3ae specification
- Passed UNH MAC, Flow-Control, Reconciliation and Inter-Operability tests
- Can be dynamically configured for NIC (Network Interface Card) applications or Switching / Bridging applications
- Standard preamble and SFD (Start of Frame delimiter) insertion and deletion with optional insertion of a user specific 8-Byte preamble
- Lane, data alignment, PHY error and local/remote fault signaling handled by the Core's Reconciliation sub-layer
- Optional MAC address comparison on receive and overwrite on transmit for NIC applications with programmable promiscuous mode operation
- Optional Multicast address filtering with 64-bin hash code lookup table on receive reducing processing load on higher layers
- Optional Ethernet Pause Frame (802.3 Annex 31A) termination providing fully automated flow control without any user application overhead
- Optional automatic Pause Frame generation from programmable FIFO congestion thresholds or by dedicated command pin with programmable Quanta
- Programmable frame maximum length providing support for any frame (e.g. Jumbo Frame or any tagged Frame)
- Support for VLAN tagged frames according to IEEE 802.1Q specification in both transmit and receive
- Dynamic inter packet gap (IPG) calculation for WAN applications
- Deficit Idle Counter (DIC) for optimized performance with minimum IPG for LAN applications
- Clock and data rate decoupling with programmable asynchronous FIFOs
- Status word available with each Frame on the User interface providing information such as frame length, VLAN Frame type indication and error information
- Preamble and SFD (Start of Frame delimiter) insertion and deletion
- Optional statistics 32-Bit or 64-Bit counters for IEEE 802.3 basic and mandatory Management Information Database (MIB) package as well as Ethernet MIB (RFC 2665) and Remote Network Monitoring (RFC 2819)

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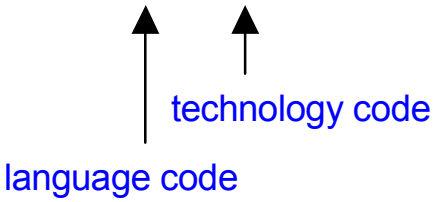
Implementation Summary

Xilinx FPGA Implementation Summary

Core Specifics		
Supported Device Family	Virtex-5 LXT Virtex-5 LX	
Version	3.1	
Resources Used		
	Min	**Max**
LUTs	3,400	6,050
FFs	3,720	6,150
Block RAM	10	User Setting Dependent
Provided with Core		
Documentation	Datasheet, User Guide	
Design File Formats	Source RTL VHDL or Verilog Encrypted RTL VHDL or Verilog	
Constraints File	UCF File	
Verification	VHDL or Verilog Self-Checking Testbench	
Supported Design Tools		
Xilinx Tool	9.1i or Later	
Simulation	Modelsim 5.7 or Later	
Synthesis	XST	
Required Speed Grade		
-1		

Ordering Code

MTIP-10GMAC-lang-tech



Language Code	*Delivery Language*
VHDL	Synthesizable RTL VHDL Source Code.
VLOG	Synthesizable RTL Verilog Source Code.
BIN	Encrypted RTL for Xilinx FPGA technology.

Technology Code	*Target Technology*
GEN	Generic sythesizable code for ASIC or FPGA implementations
XLNX	Synthesizable code optimized Xilinx FPGAs.

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