AnySpeed Ethernet MAC Core

Version 1.2 - Agust 2007

Introduction

Ethernet is available in different speeds (10/100/1000 and 10000Mbps) and provides connectivity to meet a wide range of needs from desktop to switches. MorethanIP IP solutions provide a solution for each Ethernet application with a library of configurable MAC (Media Access Control) and PCS (Physical Coding Sub-layer) Cores.

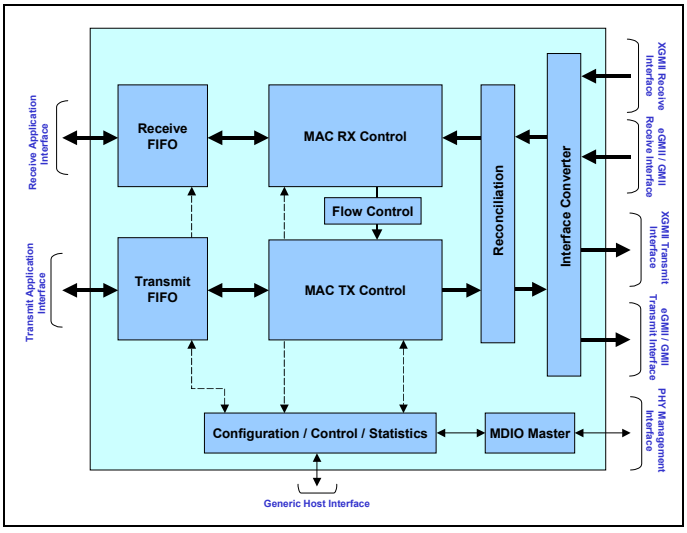
The programmable 10/100/100/10000 AnySpeed Ethernet MAC from MorethanIP provides, with a single IP Core, a solution for Ethernet applications (Line Card, NIC card or switching) operating at 10/100/1000Mbps (Gigabit Ethernet) or 10000Mbps (10 Gigabit).

The AnySpeed MAC, together with MorethanIP 1000 / 2500Base-X PCS Core can also be used to implement proprietary or industry standard 2.5Gpbs Ethernet links.

The AnySpeed MAC Core operates Full Duplex mode, supports transparent (For switching applications) and Ethernet frame termination / generation (For NIC or line cards applications) with padding and wire speed CRC check / generation.

The core can seamlessly connect to any industry standard Ethernet PHY devices via an extended 16-Bit Gigabit Medium Independent Interface for Gigabit and 2.5 Gigabit Ethernet applications and a XGMII interface for 10 Gigabit Ethernet applications.

On the Client interface, the Core implements a simple 64-Bit SOC (System on a Chip) FIFO interface which provides seamless connectivity to any MorethanIP cores or third party Cores, such as PCI-Express or SPI4.2.



AnySpeed MAC Controller Core Block Diagram

AnySpeed Ethernet MAC Core Features

- Full MAC layer and Reconciliation sub-layer implementation compliant with IEEE802.3ae specification
- Dynamically configurable to support 10 Gigabit Ethernet, with XGMII interface, Gigabit, 2.5Gbps with 16-Bit eGMII (Extended GMII) interface
- Can be configured for NIC (Network Interface Card) applications or Switching / Bridging applications
- Lane, data alignment, PHY error and local/remote fault signaling handled by the Core's Reconciliation sub-layer
- CRC-32 checking at full speed using a multi-stage CRC calculation architecture with optional forwarding of the FCS field to the user application
- CRC-32 generation and append on transmit or forwarding of user application provided FCS selectable on a per-frame basis
- Optional MAC address comparison on receive and overwrite on transmit for NIC applications
- Selectable promiscuous frame receive mode and transparent MAC address forwarding on transmit
- Optional Multicast address filtering with 64-bin hash code lookup table on receive reducing processing load on higher layers
- Optional Ethernet Pause Frame (802.3 Annex 31A) termination providing fully automated flow control without any user application overhead
- Optional automatic Pause Frame generation from programmable FIFO congestion thresholds or by dedicated command pin with programmable Quanta
- Programmable frame maximum length providing support for any frame (e.g. Jumbo Frame or any tagged Frame)
- Support for VLAN tagged frames according to IEEE 802.1Q specification in both transmit and receive
- Dynamic inter packet gap (IPG) calculation for WAN applications
- Deficit Idle Counter (DIC) for optimized performance with minimum IPG for LAN applications
- Clock and data rate decoupling with programmable asynchronous FIFOs
- Simple 64-Bit User application interface
- Optional 802.3 basic and mandatory managed Objects statistic counters and IETF Management Information Database (MIB) package (RFC2665) and Remote Network Monitoring (RMON) counters

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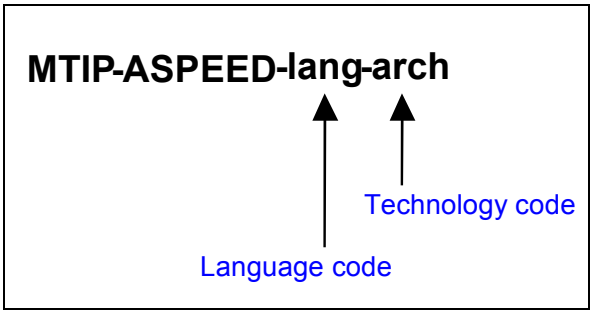
Implementation Summary

Xilinx FPGA Implementation Summary

Core Specifics		
Supported Device Family	Virtex-5LXT / Virtex-5LX	
Version	2.0	
Resources Used		
	Min	**Max**
LUTs	3650	5,960
FFs	3580	5,360
Block RAMs	9	User Settings Dependent
Provided with Core		
Documentation	Datasheet, User Guide	
Design File Formats	RTL Verilog, NGC Netlist	
Constraints File	UCF File	
Verification	Verilog Self-Checking Testbench	
Supported Design Tools		
Xilinx Tool	9.1i or Later	
Simulation	Modelsim 5.7 or Later	
Synthesis	XST	
Application Support		
Application	**Required Speed Grade**	
10 Gigabit Ethernet	-1	
2.5 Gigabit Ethernet	-1	
Gigabit Ethernet	-1	

Ordering Information



Language Code

Language Code	**Delivery Language**
BIN	Encrypted VHDL / Verilog Sources Code for Xilinx FPGAs.
VHDL	Synthesizable generic VHDL source code for Xilinx FPGA or ASICs implementations
VLOG	Synthesizable generic Verilog source code for Xilinx FPGA or ASIC implementations

Technology Code

Technology Code	**Technology**
GEN	Source code option for FPGA, Structured ASICs and ASICs.
XLNX	Encrypted RTL for Xilinx FPGAs.

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