**Product Brief**
Version 2.2 - August 2004

# 1 Introduction

Initially, 10 Gigabit Ethernet (10 GbE) is used by network managers to provide high-speed, local backbone interconnection between large-capacity switches, as it enables Internet Service Providers (ISPs) and Network Service Providers (NSPs) to create very high-speed links at a very low cost, between co-located, carrier-class switches and routers. Now, the technology also allows the construction of MANs and WANs, which connect geographically, dispersed LANs between campuses or points of presence (PoPs). These networks use dark fiber, dark wavelengths, or SONET (synchronous optical network) connections. 10 Gigabit Ethernet (10 GbE) provides compatibility with the installed OC-192 SONET rings for MAN and WAN.

As the demand for bandwidth increases, 10 GbE will be deployed throughout the entire network, and will soon include server farms, backbones, and campus-wide connectivity.

Ethernet provides significant advantages compared to other technologies, such as ATM.
10 Gigabit Ethernet extends the capabilities to WAN and MAN connectivity of lower rates Ethernet links (10/100 and Gigabit) to build end-to-end Ethernet networks with proven, simple and low cost solutions. The advantages of Ethernet compared to ATM are the following:

- No expensive, bandwidth-consuming conversion between Ethernet frames and ATM cells is required. The network is fully Ethernet, end-to-end.
- The combination of Intellectual Property (IP) and Ethernet offers the same quality of service and traffic policing capabilities as ATM, so that advanced traffic engineering technologies are available to users and providers.
- A wide variety of standard optical interfaces (wavelengths and link distances) have been specified for 10 Gigabit Ethernet, optimizing its operation and costs for LAN, MAN, and WAN applications.

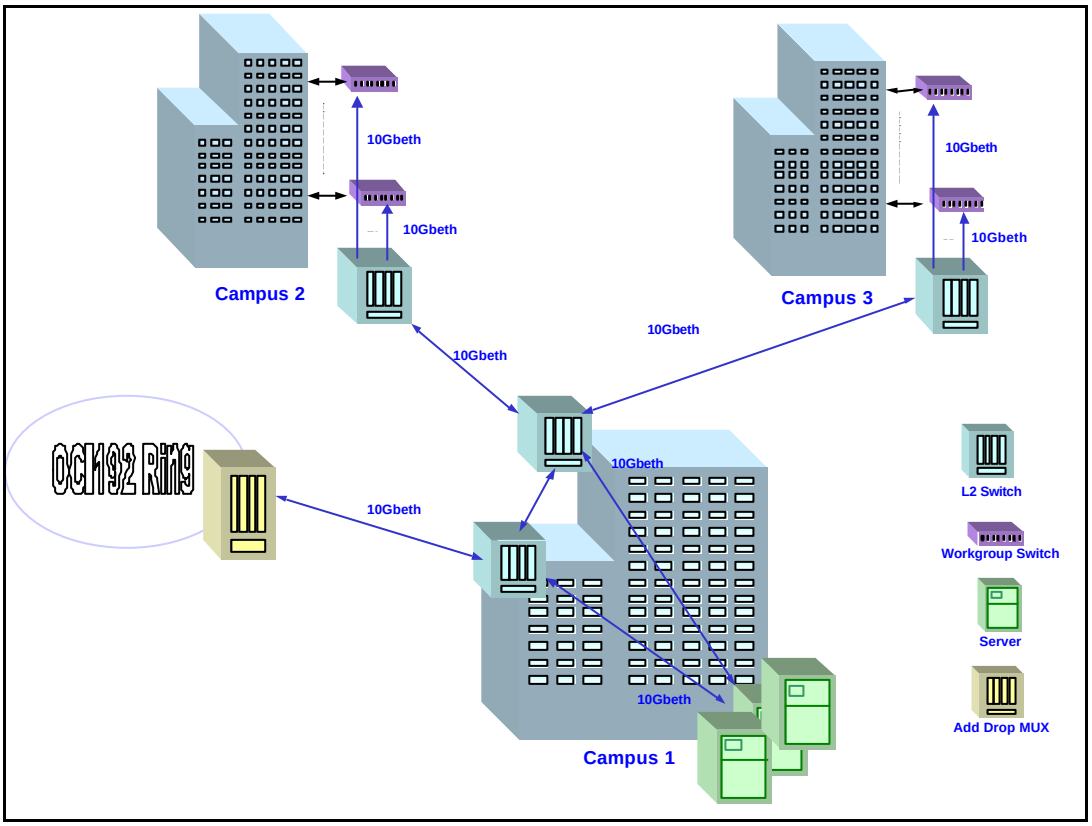


**Figure 1: 10 GbE Deployment Example**

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MorethanIP *10 Gigabit Ethernet Physical Coding Sub-Layer Core (10Base-R PCS Core)* is part of a family of cores for 10 Gigabit Ethernet applications (e.g. MAC, POS-PHY L4, Flexbus-4 and MDIO Cores). It is designed to be used in conjunction with the MorethanIP 10 Gigabit Cores to create flexible system solutions for 10 Gigabit Ethernet LAN, MAN and WAN applications.

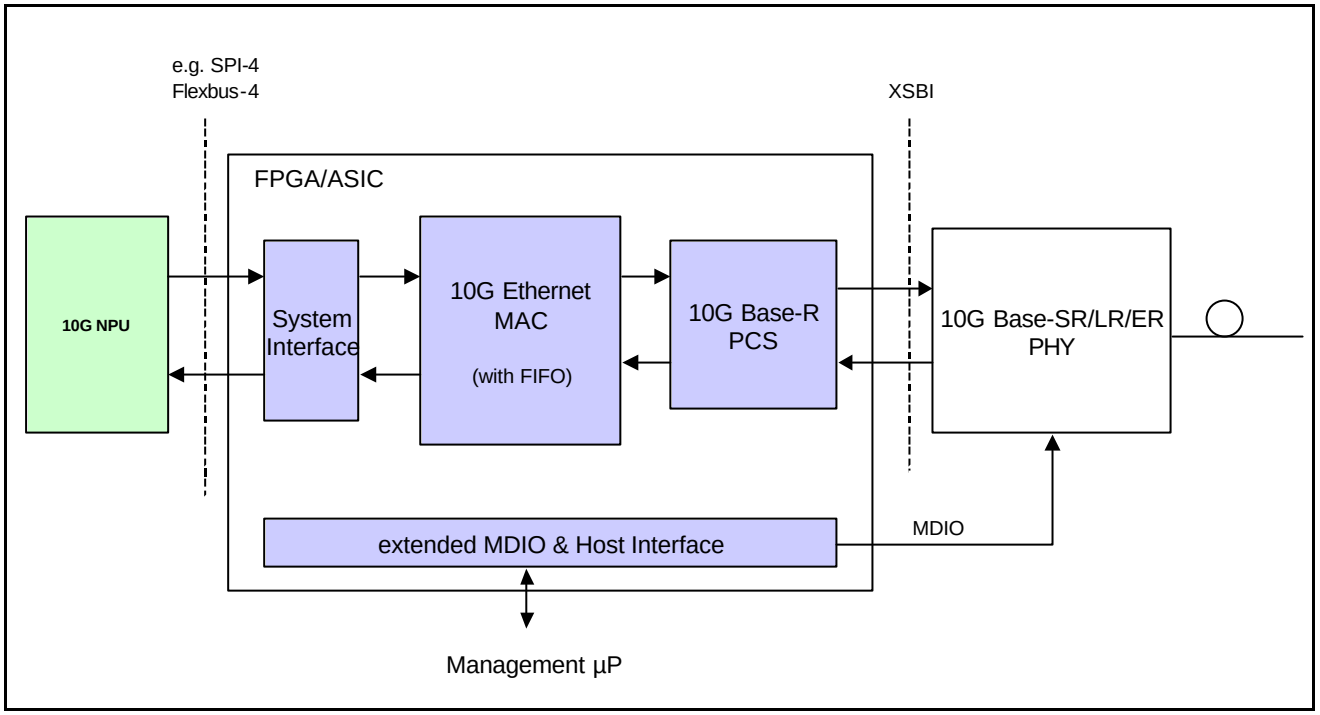


**Figure 2: 10G Ethernet Serial LAN System Solution**

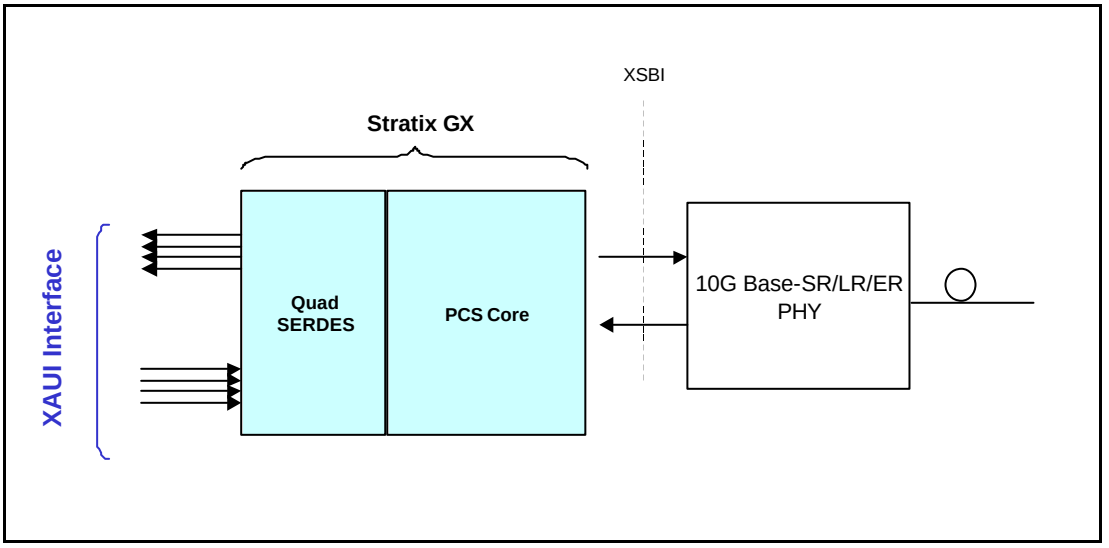


**Figure 3: XAUI Integrated Solution (Xenpak Module)**

# 2 10 Gigabit Ethernet 10GBase-R PCS Core Description

The 10GBase-R PCS core includes the 10 GbE scrambler/descrambler, the 64b/66b encoder/decoder, block synchronization and gearbox as well as clock and rate decoupling elastic buffers (FIFO).

On the application side, the Core can be configured to implement either a XGMII (10 Gigabit Medium Independent Interface) or a XAUI (10 Gigabit Attachment Unit Interface) when the design is targeted to Altera Stratix GX FPGA. Typically, the XGMII interface is selected when the Core is integrated, together with custom logic, in a FPGA or an ASIC solution while the XAUI interface provides a simpler 16-Bit board level interface to connect the PCS Core to a MAC device.

On the line side, the MorethanIP 10Gbase-R PCS Core, implements a 64-Bit interface which is typically connected, via a SFI Mux / Demux, to a XSBI interface operating at 644.53 MHz. The SFI Mux / Demux is implemented with Stratix / Stratix GX / Stratix-II high speed LVDS I/O Macros.

For use within LAN/WAN applications, with the PCS attached directly to the Transceiver Module, test pattern generator and checker are optionally implemented.

The 10Gbase-R PCS Core is compliant to IEEE[1] 802.3ae standard specification.

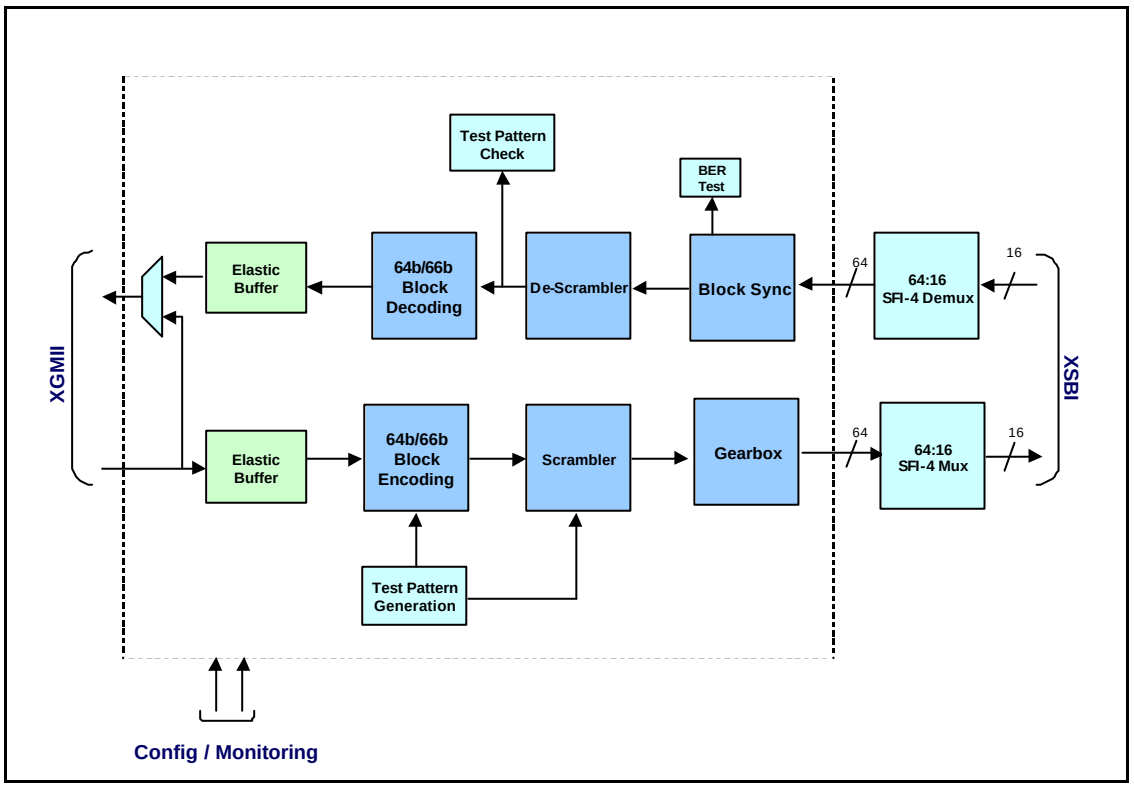


**Figure 4: 10G Base-R PCS Block Diagram**

[1] IEEE is a registered trademark of The Institute of Electrical and Electronics Engineers, Inc.

## 3 Core Features

- Complete 10GBase-R PCS solution compliant with Clause 49 of IEEE802.3ae specification
- Can be used in any 10 Gigabit Ethernet PHY applications such LAN (Local Are Network) / WAN (Wide Area Network) PHYs or in integrated 10 Gigabit Ethernet controller devices
- Optional Media independent 64-Bit non-DDR Interface or 32-Bit XGMII DDR to a 10 Gigabit Ethernet MACs or a high speed SERDES
- Optional XAUI interface implemented with Stratix GX embedded Quad SERDES providing an efficient board level interface to optical modules and loopback
- Implements 4:1 XBSI Mux / Demux when selected technology is Altera FPGA
- Implements 10 Gigabit Ethernet data Scrambler which generates a transition rich signals to the application high speed optical link and data De-Scrambler on the Core receive path
- 64/66b data coder / decoder with synchronization bit insertion / deletion on transmit / receive respectively
- 66b block synchronization on the PCS receive path and 64b block encoding on transmit with gearbox function
- 64b/66b Encoder/Decoder performing 66-bit word alignment, the 64b/66b receive path decoding, the 64b/66b transmit path encoding, and the 66b/64b transmit path conversion for block overhead bits.
- Implements XGMII / XSBI clock rates decoupling with elastic buffers on the transmit and receive paths
- Rate Matching FIFOs with idle insertion/removal allowing fully decoupled clocks of XGMII and XSBI side, simplifying system clock distribution
- Programmable loopback on the Core XGMII interface available for application test
- Implements Test Pattern Generator/Checker for link testing implemented according to IEEE 802.3ae Clause 49.2.8 and 49.2.12.
- Implement Bit Error Rate (BER) monitoring, with high error rate indication, providing constant line quality monitoring
- Can be seamlessly connected to the MorethanIP 10 Gigabit Ethernet MAC to build single chip 10 Gigabit Ethernet controller
- Optional Management Data Interface (x MDIO). The serial management interface (SMI) provides access to the internal registers of the PCS according to the Clause 45 definition of extended MDIO of 802.3ae.
- Available for Altera Stratix, Stratix GX and Stratix-II FPGAs.
- Complete design kit which includes behavioral Ethernet frame generators and checking models, PCS traffic generation model, standard compliance scenario and implementation scripts

# 4 Implementation Summary

**Table 1: Altera Stratix / Stratix GX / Stratix-II Implementation Summary**

| *Device* | *Complexity* | | *Max. Freq.* |
|---|---|---|---|
| | *Logic Elements* | *Memory Bits* | |
| Stratix | 5300 | 7008 | >161.13MHz (-C6) |
| Stratix GX | 5300 | 7008 | >161.13MHz (-C6) |
| Stratix-II | 5100 | 7008 | >161.13MHz (-C5) |

# 5 Design Package and Support

- Delivered, optionally, as an Altera FPGA netlist or in Register Transfer Level (RTL) synthesizable VHDL / Verilog source code
- Configurable VHDL / Verilog verification test-benches for automated design testing
- Scripts for Exemplar Leonardo Spectrum synthesis tools
- Script for Altera Quartus-II implementation software
- Detailed user's and methodology guides

# 6 Ordering Information

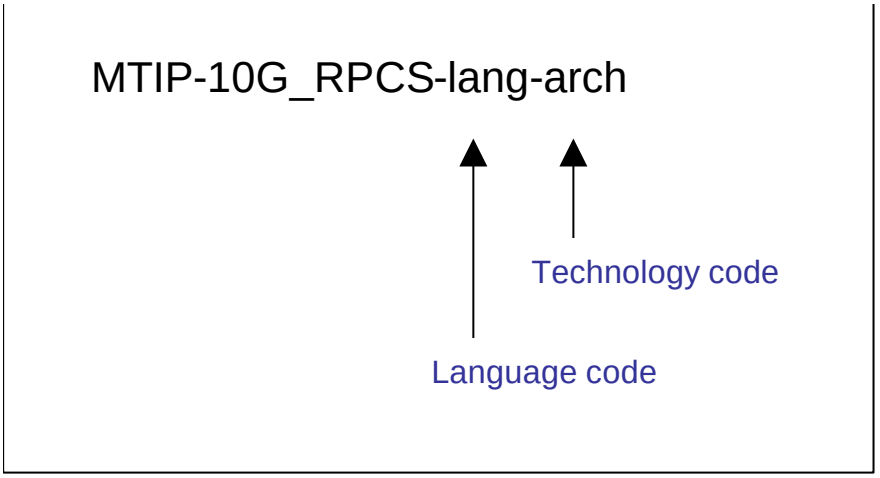


**Table 2: Language Code**

| *Language Code* | *Delivery Language* |
|---|---|
| VHDL | Synthesizable RTL VHDL. |
| VLOG | Synthesizable RTL Verilog. |
| BIN | Encrypted FPGA Netlist. |

**Table 3: Technology Code**

| *Technology Code* | *Target Technology* |
|---|---|
| GEN | Fully generic sythesizable code for ASIC or Altera Stratix, Stratix GX, Stratix-II FPGA implementations. |
| ALTR | Netlist for Altera Stratix, Stratix GX or Stratix-II FPGA implementations. |

# 7 Contact

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