

Introduction

The 10GBase-KR PCS Core includes all the functions, PCS, Autonegotiation, Link-Training and optionally FEC, required to design a solution compliant with the IEEE802.3ap backplane Ethernet specification.

On the application side, the Core can be configured to implement either a 64bit or 32bit XGMII (10 Gigabit Media Independent Interface).

On the line side, the Core, implements a 20-Bit interface that can be connected to a 10.3125Gbps Serdes.

The Core implements the Clause 73 Backplane Autonegotiation and Clause 72 link training function according to the IEEE802.3ap standard.

Optionally, the 10GBase-KR PCS Core can implement a Forward Error Correction (FEC) module. The FEC is compliant with the IEEE802.3ae Clause 74 and can be used to add margin to account for variations in manufacturing and environmental conditions.

The 10Gbase-KR PCS Functions are compliant to IEEE¹ 802.3ap standard specification and are UNH tested, when available.

The core is delivered in generic Source or Encrypted Verilog synthesizable HDL code.

10GBase-KR PCS Core Features Overview

PCS

- Compliant with the IEEE802.3ae Clause 49 specification
- Media independent 64-Bit or 32-Bit non-DDR XGMII Interface to the MAC
- Implements 10 Gigabit Ethernet 64/66b data coder / decoder scrambler and block synchronization
- Gearbox functions to allow flexible bit width on serdes interfaces
- Implements XGMII / Line clock rates decoupling with elastic buffers on the transmit and receive paths
- Implements Test Pattern Generator/Checker for link testing implemented according to IEEE 802.3ae Clause 49.2.8 and 49.2.12.
- Implement Bit Error Rate (BER) monitoring, with high error rate indication, providing constant line quality monitoring
- Optional support for 802.3az Energy Efficient Ethernet (EEE) applications

Optional FEC

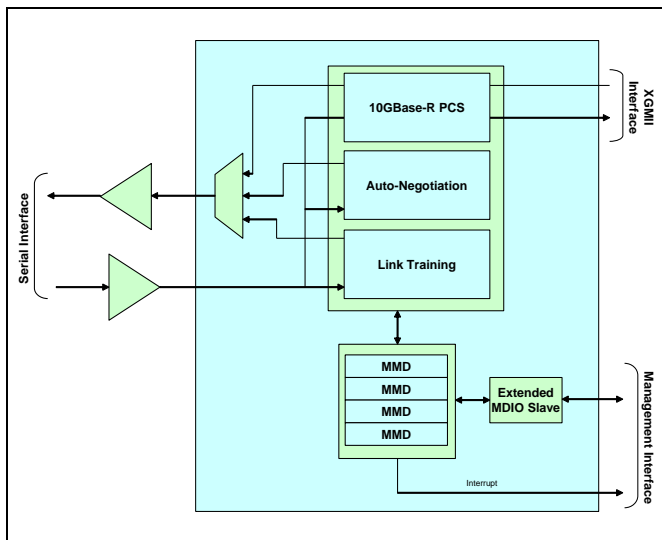
- FEC(2112, 2080) Core compliant with the IEEE802.3ae Clause 74 specification.
- Low Latency avoiding inverse gearbox functions
- Fast-Lock support for use with 802.3az Energy Efficient Ethernet (EEE) applications

Auto-Negotiation

- Compliant with Clause 73 of the IEEE802.3ap specification
- Support auto-negotiation with automatic technology selection (only 10G Base-R supported)
- Ability page from Link partner is visible to the management interface after successful negotiation
- Next Page exchange after the Base Page exchange possible under application control to exchange any messages as needed.
- Can be software disabled for non-backplane 10GBase-R applications

Link Training / Startup Protocol

- Compliant with Clause 72 for 10G Base-KR PMD of the IEEE802.3ap specification
- Training fully application controlled
- Can be software disabled for non-backplane 10GBase-R applications



10GBase-KR PCS Core Block Diagram

¹ IEEE is a registered trademark of The Institute of Electrical and Electronics Engineers, Inc.

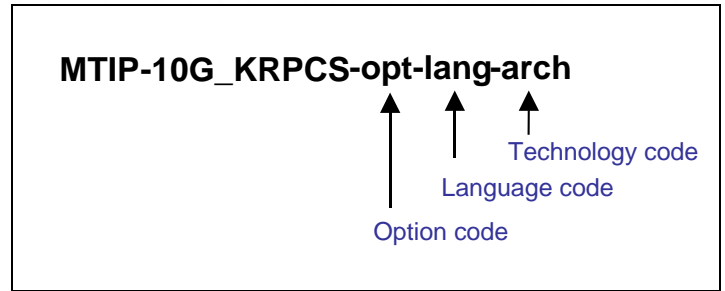
Management Interface

- Implements a MDIO Slave interface compliant with the IEEE 802.3 Clause 45
- Optional direct register interface to every module
- Includes PMA/PMD, PCS, Auto-Negotiation MDIO Manageable Devices
- Implements an interrupt controller in a Vendor specific MDIO Manageable Device

Implementation Summary

Core Specifics		
Supported Device Family	any	
Resources Used		
	without FEC	with FEC
FFs	8500	9800
Memory bits	1800	4000
Deliverables		
Documentation	Reference Guide, User Guide	
Design File Formats	Source RTL Verilog or Encrypted RTL Verilog	
Constraints File	SDC Files	
Verification	Self-Checking Testbench	
Supported Design Tools		
Simulation	Modelsim 6.x or Later	
Synthesis	any	
Implementation	any	

Ordering Code



Option Code	Option
FEC	FEC functions.

Language Code	Delivery Language
VLOG	Synthesizable RTL Verilog Source Code.
BIN	Encrypted RTL for FPGA technology.

Technology Code	Target Technology
GEN	Generic synthesizable source for ASIC or FPGA implementations
ALTR	Synthesizable code optimized for Altera FPGAs.

Contact

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