Product Brief
Version 3.0 - May 2005

1 Introduction

Initially, 10 Gigabit Ethernet is used by network managers to provide high-speed, local backbone interconnection between large-capacity switches, as it enables Internet Service Providers (ISPs) and Network Service Providers (NSPs) to create very high-speed links at a very low cost, between co-located, carrier-class switches and routers. Now, the technology also allows the construction of MANs and WANs, that connect geographically dispersed LANs between campuses or points of presence (PoPs). These networks use dark fiber, dark wavelengths, or SONET (synchronous optical network) connections. 10 Gigabit Ethernet provides compatibility with the installed OC-192 SONET rings for MAN and WAN with 10Gbase-W PHY interfaces.

As the demand for bandwidth increases, 10 Gigabit Ethernet will be deployed throughout the entire network, and will soon include server farms, backbones, and campus-wide connectivity.

Ethernet provides significant advantages compared to other technologies, such as ATM.
10 Gigabit Ethernet extends the capabilities to WAN and MAN connectivity of lower rates Ethernet links (10/100 and Gigabit) to build end-to-end Ethernet networks with proven, simple and low cost solutions. The advantages of Ethernet compared to ATM are the following:

- No expensive, bandwidth-consuming conversion between Ethernet frames and ATM cells is required. The network is fully Ethernet, end-to-end.
- The combination of Intellectual Property (IP) and Ethernet offers the same quality of service and traffic policing capabilities as ATM, so that advanced traffic engineering technologies are available to users and providers.
- A wide variety of standard optical interfaces (wavelengths and link distances) have been specified for 10 Gigabit Ethernet, optimizing its operation and costs for LAN, MAN, and WAN applications.

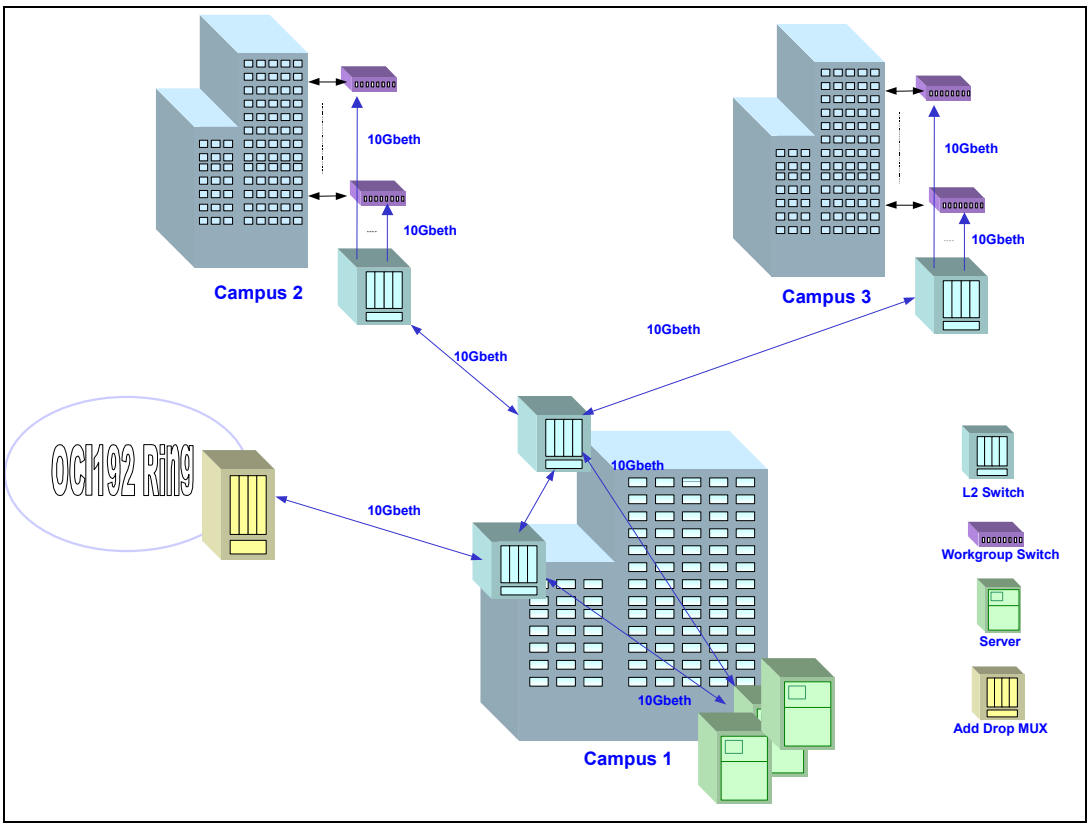

Figure 1: 10 Gigabit Ethernet Deployment Example

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The 10Gbase-W PHY specification defines a PHY, which has a data rate compatible with payload rate of OC-192c SONET rings. The 10Gbase-W PHY enables the use SONET infrastructure for Layer 1 transport and therefore requires, together with a 10 Gigabit Ethernet PCS (Physical Coding Sub-Layer), which implements frame delineation and scrambling, the implementation of a reduced specification SONET framer.

The MorethanIP 10GBase-R / W PHY Core is part of a family of Cores for 10 Gigabit Ethernet applications. The 10GBase-W PHY combines the MorethanIP proven 10 Gigabit PCS (Physical Coding Sub-Layer) Core with MorethanIP OC-192 SONET Core. The 10GBase-W Core is available on Altera Stratix or Stratix-II FPGAs and, with a XAUI MAC interface, on Stratix GX and Stratix II GX FPGAs.

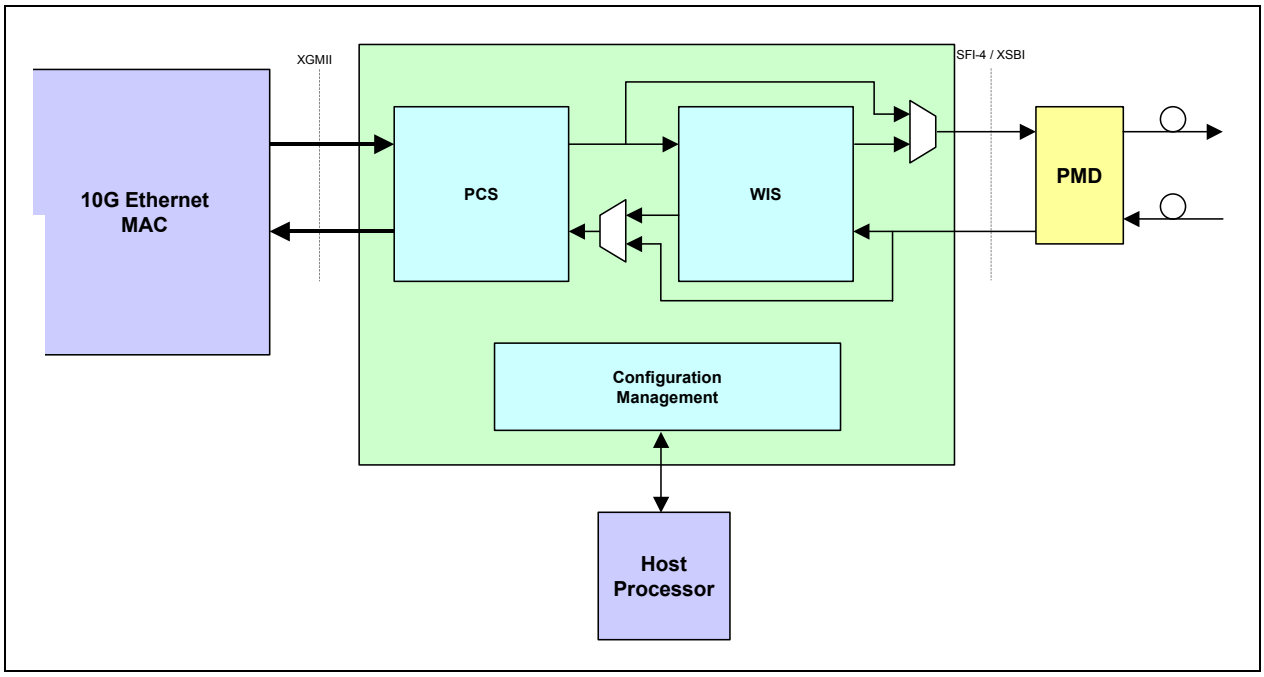

Figure 2: Core Application – 10-Gigabit Programmable PHY

2 10 Gigabit Ethernet 10Gbase-R / W PHY Core Description

The 10GBase-R PCS core includes the 10 Gigabit Ethernet scrambler/descrambler, the 64b/66b encoder/decoder. The Core optionally implement a 32-Bit DDR (Double Data Rate) 10 Gigabit Ethernet Media Independent short-reach XGMII Interface or a 64-Bit data interface.

The WIS (WAN Interface Sub-Layer), connected to the PCS Core, is implemented with Altera OC192 SONET framer Magacore. The WIS sub-layer maps the frames from the 10 Gigabit PCS in a SONET payload, adds the SONET overhead bytes and performs SONET line scrambling. In addition, the WIS sub-layer provides OAM services via registers, for example, to an external processor.

On the line side, the 10Gbase-W PHY Core implements a 64-Bit interface which is typically connected, via a SFI-4 Mux / Demux, to a PMD (Physical Medium Dependent) device. The SFI-4 Mux / Demux can be implemented with Stratix high speed LVDS I/O Macros.

The MorethanIP PCS Core and OC-192 SONET Framer Core are combined together, via a common MidBUS interface, in a single programmable chip solution with Altera FPGAs or Structured ASICs, which provides significant time to market advantage.

Optionally the Core can be combined with MorethanIP 10 Gigabit MAC Core if a large-scale integration is required. The 10Gbase-W PHY Core is compliant to IEEE[1] 802.3ae standard.

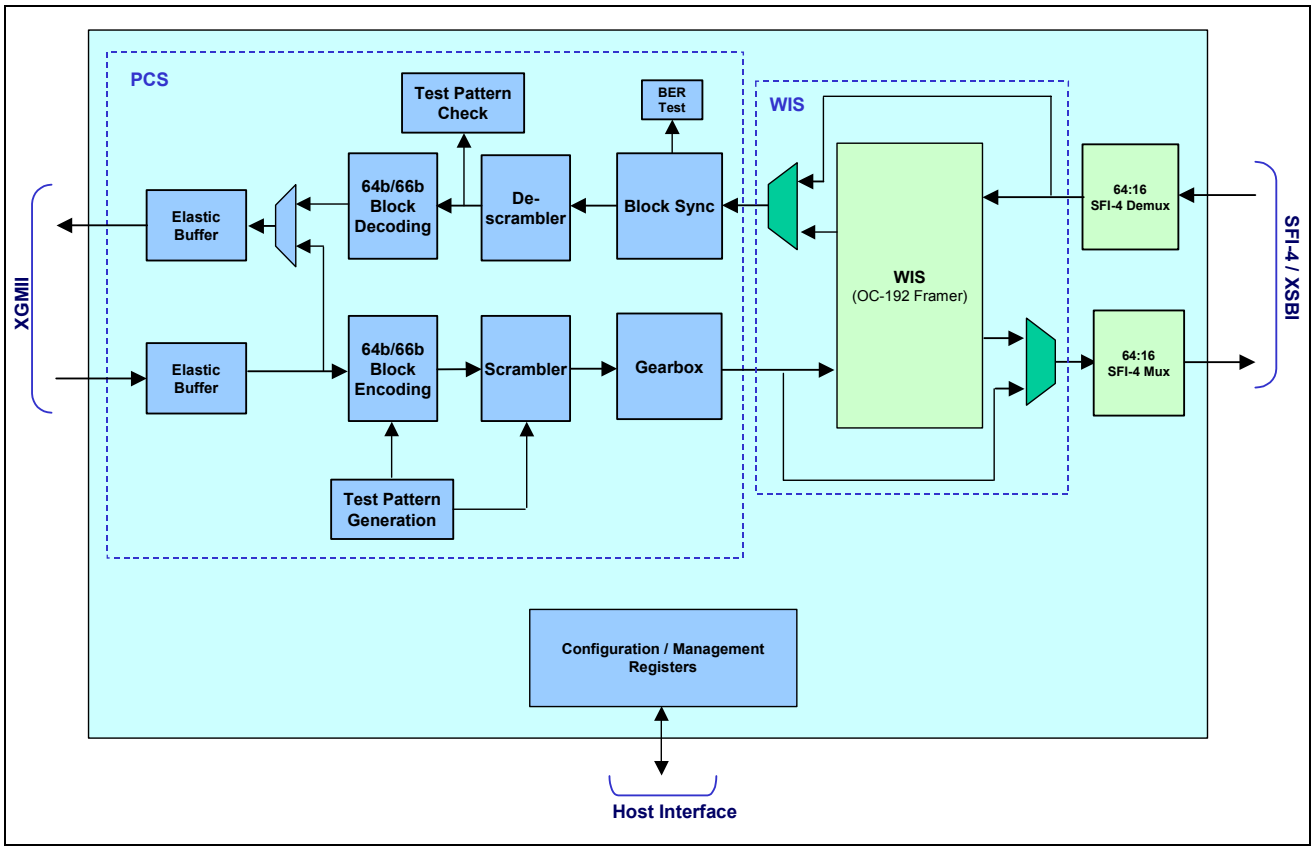

Figure 3: 10GBase-R / W PCS Core Block Diagram

[1] IEEE is a registered trademark of The Institute of Electrical and Electronics Engineers, Inc.

3 Features

- Compliant with the IEEE802.3ae specification Clauses 49 (Physical Coding Sublayer (PCS) for 64B/66B) and Clause 50 (WAN Interface Sub-Layer (WIS))
- Dynamically programmable to support 10GBase-R (IEEE802.3ae Clause 49) or 10GBase-W 10 Gigabit Ethernet PCS operation
- Implements 10 Gigabit PCS Layer and WIS Sub-Layer that can be by-passed if the Core operates in 10GBase-R Mode
- Optional Media independent 64-Bit non-DDR Interface XGMII DDR or to a 10 Gigabit Ethernet MACs or a high speed SERDES
- Implements 10 Gigabit Ethernet data Scrambler which generates a transition rich signals to the application high speed optical link and data De-Scrambler on the Core receive path
- 64/66b data coder / decoder with synchronization bit insertion / deletion on transmit / receive respectively
- 66b block synchronization on the PCS receive path and 64b block encoding on transmit with gearbox function
- 64b/66b Encoder/Decoder performing 66-bit word alignment, the 64b/66b receive path decoding, the 64b/66b transmit path encoding, and the 66b/64b transmit path conversion for block overhead bits.
- Implements XGMII / WIS clock rates decoupling with elastic buffers and Idle stuffing / de-stuffing on the transmit and receive paths
- Programmable internal loopback
- Implement Bit Error Rate (BER) monitoring, with high error rate indication, providing constant line quality monitoring
- Implements programmable Square Wave test-pattern generation and checking that can be used when the Core operates in 10GBase-R Mode
- Implements PRBS31 pseudo-random pattern generation for Transmit line and CDR performance testing
- Implements Test Pattern Generator/Checker for link testing implemented according to IEEE 802.3ae Clause 49.2.8 and 49.2.12.
- Can be seamlessly connected to the MorethanIP 10 Gigabit Ethernet MAC to build single chip 10 Gigabit Ethernet controller
- WIS Framer implements full pointer processing, BIP generation checking, Line and Path trace insertion and extraction
- Direct interface to optical transponder with a 16-Bit SFI-4 / XSBI interface
- Parallel 32-Bit management and configuration interface
- WIS Framer configuration and status check via Core management interface
- Can be seamlessly connected to the MorethanIP 10 Gigabit Ethernet MAC to build single chip 10 Gigabit Ethernet controller
- Available for Stratix-II, Stratix, StratixGX and Stratix II GX FPGAs

4 Implementation Summary

Table 1: Implementation Summary

Device	*Complexity*	
	Logic Elements	*Memory Bits*
Stratix / Stratix GX	17000LEs	200K
Stratix II / Stratix II GX	15000LEs	200K

5 Contact

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