Product Brief
Version 1.1 - April 2005

1 Introduction

Initially, network managers use 10 Gigabit Ethernet to provide high-speed, local backbone interconnection between large-capacity switches. 10 Gigabit Ethernet enables Internet Service Providers (ISPs) and Network Service Providers (NSPs) to create very high-speed links at a very low cost, between co-located, carrier-class switches and routers. The technology also allows the construction of MANs and WANs that connect geographically dispersed LANs between campuses or points of presence (PoPs). These connections use dark fiber, dark wavelengths, or SONET (synchronous optical network) networks. 10 Gigabit Ethernet provides, for MAN and WAN, compatibility with the installed OC-192 SONET rings.

As the demand for bandwidth increases, 10 Gigabit Ethernet will be deployed throughout the entire network, and will include server farm, backbone, and campus-wide connectivity.

Ethernet provides significant advantages over other technologies, such as ATM. 10 Gigabit Ethernet extends the capabilities, to WAN and MAN connectivity, of lower rates (10/100 and 1Gbps) Ethernet links to build end to end Ethernet networks with proven, simple and low cost solutions:

- No expensive, bandwidth-consuming conversion between Ethernet frames and ATM cells is required; the network is Ethernet, end to end.
- The combination of IP and Ethernet offers Quality of Service and traffic policing capabilities that approach those provided by ATM, so that advanced traffic engineering technologies are available to users and providers.
- A wide variety of standard optical interfaces (wavelengths and link distances) have been specified for 10 Gigabit Ethernet, optimizing its operation and cost for LAN, MAN, or WAN applications.

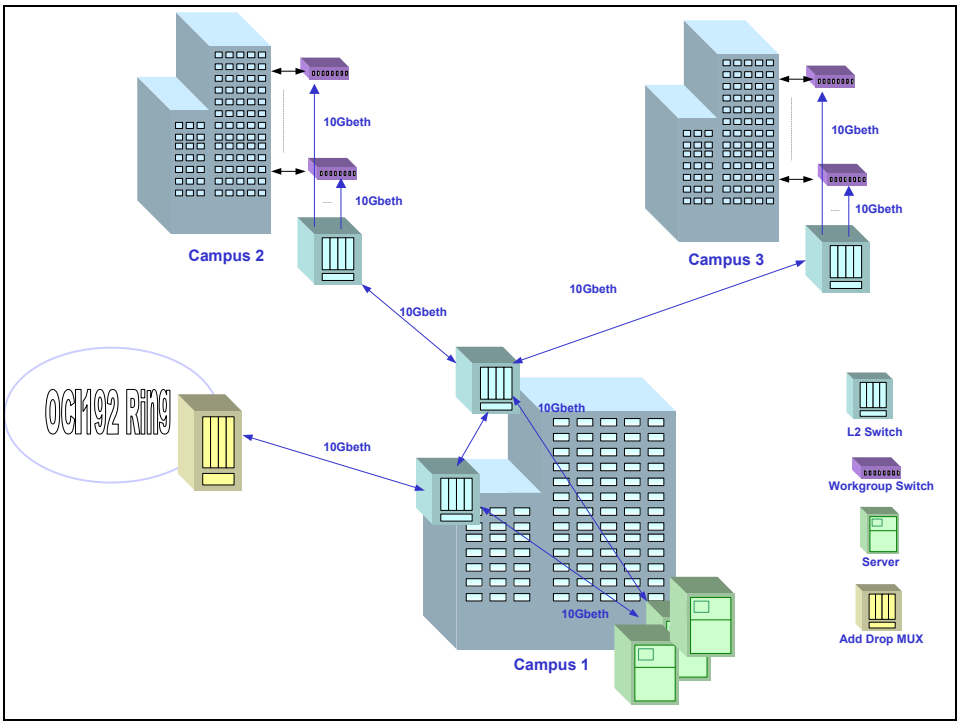

Figure 1: 10 Gigabit Ethernet Deployment Example

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XAUI (10 Gigabit Attachment Unit Interface) provides a low pin count board level interface to connect a 10 Gigabit Ethernet MAC to a physical device such as an optical transponder or Xenpack, XPAK or X2 modules. Using a XAUI interface (rather than XGMII) on a 10 Gigabit MAC application simplifies the board design and allows extension of distance between MAC and PHY layer over e.g. backplanes or implementing connectors for pluggable PHY modules.

The XGXS (10 Gigabit Extension Sub-Layer) PCS (Physical Coding Sub-Layer) Core is designed to comply with the IEEE802.3ae Clause 48 and can be used, together with MorethanIP 10 Gigabit Ethernet MAC Core, to implement a 10 Gigabit Ethernet solution with a XAUI.

The XGXS Core implements and interface between a 64-Bit de-multiplexed XGMII interface or a standard DDR (Dual Data Rate) and, in combination with a Quad-3.125 Gbps SerDes, a XAUI interface that provides a low pin-count board level interface.

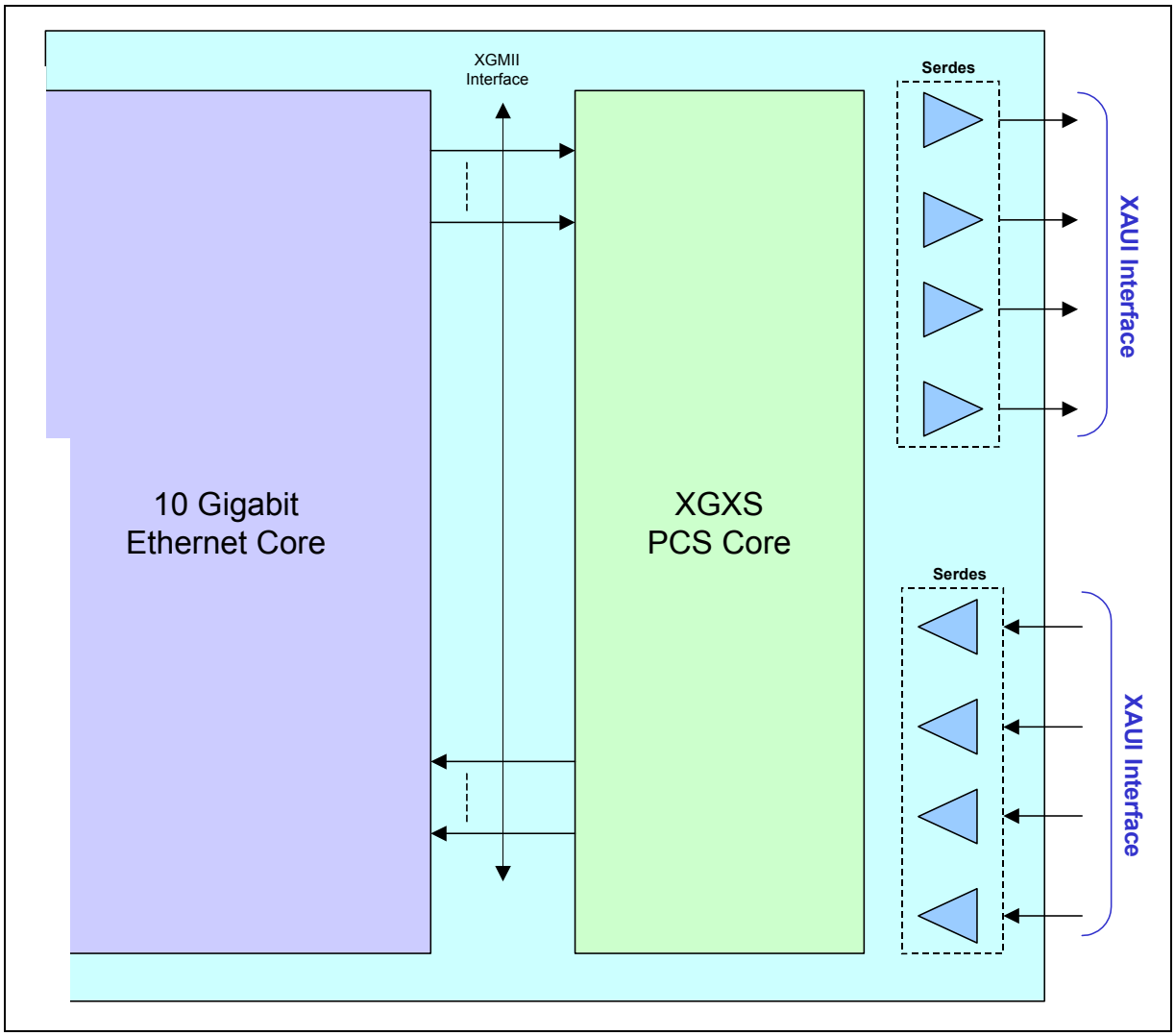

Figure 2: 10 Gigabit Ethernet MAC with XAUI Application Example

2 10 Gigabit Ethernet XGXS PCS Core Features Overview

- XGXS PCS function compliant with the IEEE802.3ae Clause 48 specification
- Implements XGXS PCS frame encapsulation / de-encapsulation with Start, Terminate ordered set insertion / termination and Randomized Idle ordered set generation during inter-packet gap
- Implements receive link synchronization state machine and 10-Bit data alignment from SERDES with Comma character detection
- Link coding implemented with 8B/10B providing DC balanced bitstream for efficient SERDES operation
- Implements a 64-Bit XGMII interfaces that can be seamlessly connected to MorethanIP 10 Gigabit Ethernet MAC Core
- Rate matching to adapt Rates from the XAUI Line clock with the XGMII Receive Clock
- Link coding implemented with 8B/10B providing DC balanced bitstream for efficient SERDES operation
- Implements a link synchronization state machine per port
- Receive Lane alignment (Deskew) designed to compensate XAUI lines skew
- Can be implemented in Altera FPGAs, Altera Hardcopy devices, Structured ASICs or ASICs
- Can optionally be delivered in VHDL or Verilog source code or netlist which provides a lower cost licensing option
- Design Kit contains extensive Ethernet frame generators and checking models enabling fully automated design verification and testing for standard compliance and error behavior, enabling for fast turn-around design cycles

3 10 Gigabit Ethernet XGXS Core Block Diagram

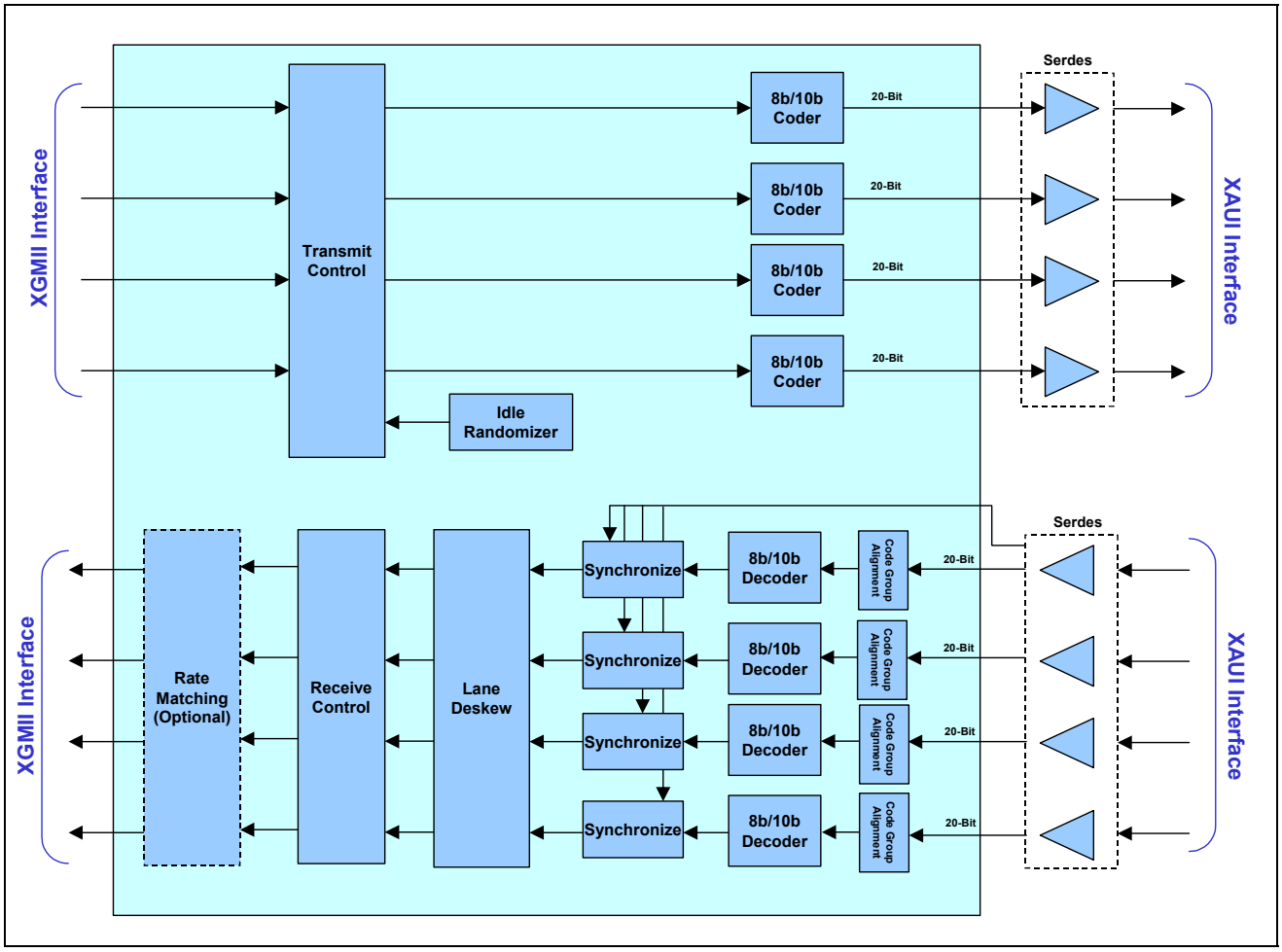

Figure 3: 10 Gigabit Ethernet XGXS Core Block Diagram

4 Implementation Summary

Table 1: FPGA Implementation Summary

Target Device Family	Speed Grade	Complexity (With Rate Matching FIFO)		Performance	Minimum Requirement
		LEs	RAM bits		
STRATIX-II	-5	4000 (ALUT)	3500	160 MHz	156.25MHz

Table 2: ASIC Implementation Summary

Process Technology	*Process Geometry*	*Complexity (Gates)*	*Area (um^2)*	*Maximum clock frequency (MHz)*	*Slack for critical path*
CLN90G	90nm	48000	130079.49	426.25	+5.655ns
CL011LVP	0.11um	54000	265159.53	511.00	+6.043ns
CL013G	0.13um	54000	265015.09	335.50	+5.021ns
CL015G	0.15um	54500	381147.35	562.25	+6.222ns
CL018G	0.18um	56000	537459.72	401.75	+5.512ns

Conditions:

Synthesis Tool: TeraForm
Top Metal layer: 4M
Wire load model:

Standard Cell Library Vendor: TSMC
Characterization Corner: typical (TT Process Spice Models, 1.0V, 25 Degrees C)

5 References

1. IEEE 802.3 2002 Edition
2. IEEE 802.3ae 2002 Edition

6 Contact

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