Low-Latency 10M to 10G Anyspeed Ethernet MAC Product Brief

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Introduction

The Low-Latency Anyspeed Ethernet MAC Core is designed to comply with the IEEE802.3 specifications for 10/100/1000Mbps and 10Gbps meeting the requirements for both WAN / MAN and LAN connectivity. Its flexible rate design also allows for industry standard 2.5Gbps operation.

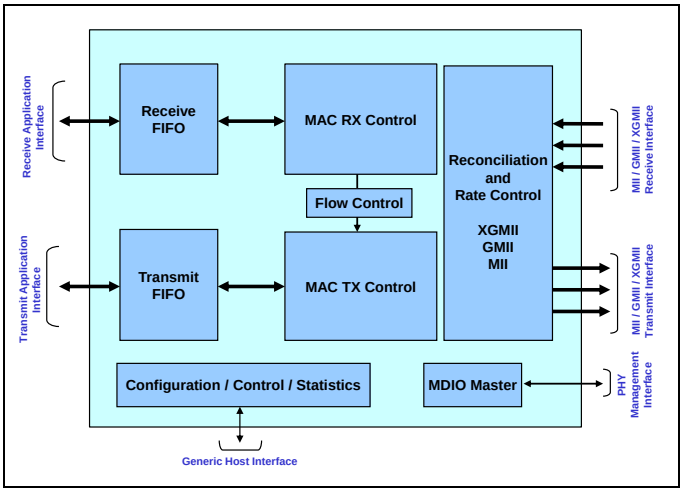
The MAC can be used in either Network Interface Card (NIC) or Ethernet Switching applications. A set of configuration registers allows to dynamically set the Core to terminate and form MAC frames (NIC application) or to pass MAC frames without modification (Switching application). The Core provides statistics support for IEEE managed objects, IETF MIB-II and RMON for management applications (e.g. SNMP).

On the Ethernet Line side, the Core implements a 32-bit XGMII (10 Gigabit Medium Independent Interface), an 8-bit GMII and a 4-bit MII. Further adaptation modules for serial and reduced variants (SMII, RMII, RGMII, SGMII, ...) can be chosen separately for supporting any available PHY interface.

The Ethernet MAC Core, on the Application side, implements a 32-bit or 64-bit asynchronous FIFO interface with a simple handshaking procedure.

With its advanced rate adapting design the MAC Core in combination with MorethanIP PCS Layer allows for very efficient and low latency implementations by avoiding rate-matching FIFOs between the MAC and PHY Layers.

The core is delivered either in generic Verilog synthesizable HDL code for ASIC and FPGA implementations, or in an encrypted format for FPGA implementations.



Anyspeed Ethernet MAC Core Block Diagram

Ethernet MAC Core Main Features Overview

- MAC and Reconciliation Sublayer implementation compliant with IEEE802.3 specifications
- Low-Latency 32-bit datapath design with flexible rate capability supporting 10/100/1000M, 2.5G and 10G
- Dynamically configurable to operate with a 32-bit XGMII (10G) or 8bit GMII (1G, 2.5G) or 4bit MII (10/100) interface
- Full-duplex line rate support at all speeds and optionally half-duplex operation for 10/100 networks
- Dynamically configurable for NIC (Network Interface Card) or Switching / Bridging applications
- Standard preamble/SFD (Start of Frame Delimiter) insertion and deletion with optional custom preamble
- Lane, data alignment, PHY error and local/remote fault signaling handled by the Core's Reconciliation sub-layer
- Optional MAC address match on receive and overwrite on transmit with programmable promiscuous mode operation
- Optional Multicast address filtering with 64-bin hash code lookup on receive reducing load on higher layers
- Ethernet Pause Frame (802.3 Annex 31B) generation and termination for automatic as well application controlled flow control
- Support for Priority Flow Control (PFC, 802.1Qbb) frames allowing control for 8 classes for congestion management.
- Programmable frame maximum length up to 32Kbyte
- Support for VLAN tagged frames according to IEEE 802.1Q specification
- Dynamic inter packet gap (IPG) calculation for LAN/WAN applications with Deficit Idle Counter (DIC) for optimized performance with minimum IPG
- Clock and data rate decoupling with programmable asynchronous FIFOs at the application interface
- Status word available with each Frame on the User interface providing information such as frame length, VLAN Frame type indication and error information
- Statistics 64-Bit counters for IEEE 802.3 basic and mandatory Management Information Database (MIB) package as well as Ethernet MIB (RFC 2665) and Remote Network Monitoring (RFC 2819)
- TX/RX Timestamping enabling IEEE 1588 applications
- Support for Energy Efficient Ethernet (EEE) 802.3az
- Integrated MDIO Master supporting both Clause 22 and Clause 45 managed PHY modules
- Optional Magic Packet detection for power management

Latency Examples

Mode (Line Freq.)	FIFO (ns)	MAC (ns)	MAC+FIFO+64 byte frame store&forward round-trip time (Time Application writes EOP to TX FIFO until EOP from RX FIFO to application)
10G XGMII (312.5MHz)	TX: 30 RX: 30	TX: 9.6 RX: 19.2	189 ns
1G GMII (125 MHz)	TX: 63 RX: 42	TX: 64 RX: 152	888 ns
100M MII (25MHz)	TX: 254 RX: 105	TX: 760 RX: 1440	7.770 µs

Note: Application side frequency is 312.5MHz for all modes shown in table above.

Implementation Summary

Target Device Family	Complexity (fullduplex only)	Memory (bits) 1024x32 TX/RX FIFOs	Performance
ASIC	~70K gates ~6000 DFFs	73K	> 650 MHz
FPGA e.g. Stratix IV,V	~4600 ALUT (~4500 DFFs)	73K	312.5MHz

Deliverables

- Verilog Synthesizable RTL or encrypted RTL for FPGA implementation
- Behavioral Verilog testbenches and Verification test cases
- Support for FPGA and ASIC design tools

Ordering Code

MTIP-10G32MGMII-lang-tech

Language Code	*Delivery Language*
VLOG	Synthesizable RTL Verilog Source Code.
BIN	Encrypted RTL for FPGA technology.

Technology Code	*Target Technology*
GEN	Generic sythesizable code for ASIC or FPGA implementations
ALTR	Synthesizable code for Altera FPGAs.
XIL	Synthesizable code for Xilinx FPGAs.

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