XS4 10 Gigabit Ethernet and HiGig / HiGig+ SPI4.2 Bridge

Product Brief
Version 1.6 - December 2006

Introduction

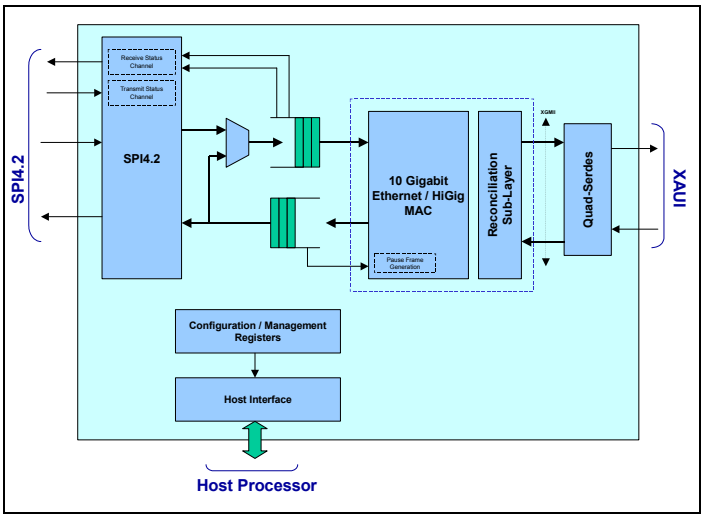
The XS4 (XAUI SPI4.2) Bridge from MorethanIP provides a cost effective and integrated solution to Bridge an SPI4.2 Interface to a XAUI interface. The XS4 Bridge provides a generic solution to meet multiple design requirements such as device Bridging (e.g. NPU to Ethernet Switch), Serial Backplane applications, Packet over SONET/SDH (POS) or Ethernet over SONET/SDH (EOS) applications.

The XS4 Bridge implements an optimized 10 Gigabit Ethernet MAC function, compliant with the IEEE802.3ae specification and UNH certified. The MAC function implements a full 10 Gigabit Ethernet reconciliation sub-layer, for frame encapsulation and compatibility with XAUI Quad SERDES and devices, IPG (Inter-Packet Gap) for correct operation with standard 10 Gigabit Ethernet devices and pause frame generation / termination for flow control across the XAUI interface.

The MAC is designed to transparently transfer frames without modification and, to provide performance monitoring on the backplane interface the MAC can optionally perform standard CRC check on every frame received from the XAUI interface. The MAC also implements a HiGig / HiGig+ mode, which can used to interface with Broadcom switches.

The SPI4.2 interface is compliant with the PMC-Sierra PMC-1991635 specification document. The interface implements a high speed 16-Bit DDR (Double Data Rate) SPI4.2 transmit / receive data path and a low speed transmit / receive FIFO status channel.

The Bridge implements a 64K-Byte FIFO on the MAC receive path (XAUI to SPI4.2 path) that provide buffering for up seven Jumbo Ethernet frames (9K Bytes frame) providing loss-less flow control across the XAUI interface.



XS4 Block Diagram

XS4 Bridge Features

10-Gigabit Ethernet / HiGig+ MAC

- Full MAC layer and Reconciliation sub-layer implementation compliant with IEEE802.3ae specification
- Optional Direct interface to standard 32-Bit DDR (Dual Data Rate) XGMII connections or to a selection of high speed SERDES devices via a 32-Bit HSTL Class I interface
- Optional XAUI interface implemented with embedded Quad SERDES providing an efficient board level interface to optical modules and loopback
- Optional HiGig / HiGig+ Mode to interface Broadcom Switch devices
- Lane, data alignment, PHY error and local/remote fault signaling handled by the Bridge Ethernet Reconciliation sub-layer
- Programmable Unicast frame filtering on receive or promiscuous mode
- Supports Multicast and Broadcast frames and SNAP, LLC and any typed frames
- Automatic discard of received errored frames with indication in specific statistic registers
- Optional forwarding of received pause frames to the Bridge SPI4.2 interface
- Optional automatic Pause Frame generation from programmable FIFO congestion thresholds or via a register command bit
- Programmable frame maximum length providing support for any frame (e.g. Jumbo Frame or any tagged Frame)
- Support for VLAN tagged frames according to IEEE 802.1Q specification in both transmit and receive
- Preamble and SFD (Start of Frame delimiter) insertion and deletion
- Programmable Preamble providing a low speed in-band communication channel

SPI 4.2 Interface

- Compliant with PMC-Sierra PMC-1991635 specification document
- Transmit and receive status channel operating at 100MHz with LVTTL compatible I/Os
- Programmable FIFO Thresholds generating the SPI4.2 Starving / Hungry and Satisfied levels
- Programmable training sequences and control
- Optional Dynamic phase alignment

Optional Host Interface

- Complete set of error event counters providing application management and application monitoring accessible via host processor interface

Implementation Summary

Table 1: Implementation Summary - Lite Version

Target Device Family	Speed Grade	Complexity	
		Total LEs	Total Memory Bits
STRATIX II	-4	8600 (1)	750K
STRATIX II GX	-4	8600 (1)	

Table 2: Implementation Summary - Full Version

Target Device Family	Speed Grade	Complexity	
		Total LEs	Total Memory Bits
STRATIX II	-4	15000 (1)	750K
STRATIX II GX	-4	15000 (1)	

1. The Logic Element count for Stratix II devices is based on the number of adaptive look-up tables (ALUTs) used for the design as reported by the Quartus II software.

Contact

MorethanIP

E-Mail : info@morethanip.com
Internet : www.morethanip.com
Muenchner Strasse 199
D-85757 Karlsfeld
Germany
Tel : +49 (0) 8131 333939 0
FAX : +49 (0) 8131 333939 1