Product Brief - PRELIMINARY
Version 1.0 - August 2005

1 Introduction

Ethernet is available in different speeds (10/100/1000 and 10000Mbps) and provides connectivity to meet a wide range of needs from desktop to switches. MorethanIP IP solutions provide a solution for each Ethernet application with a library of configurable MAC (Media Access Control) and PCS (Physical Coding Sub-layer) Cores.

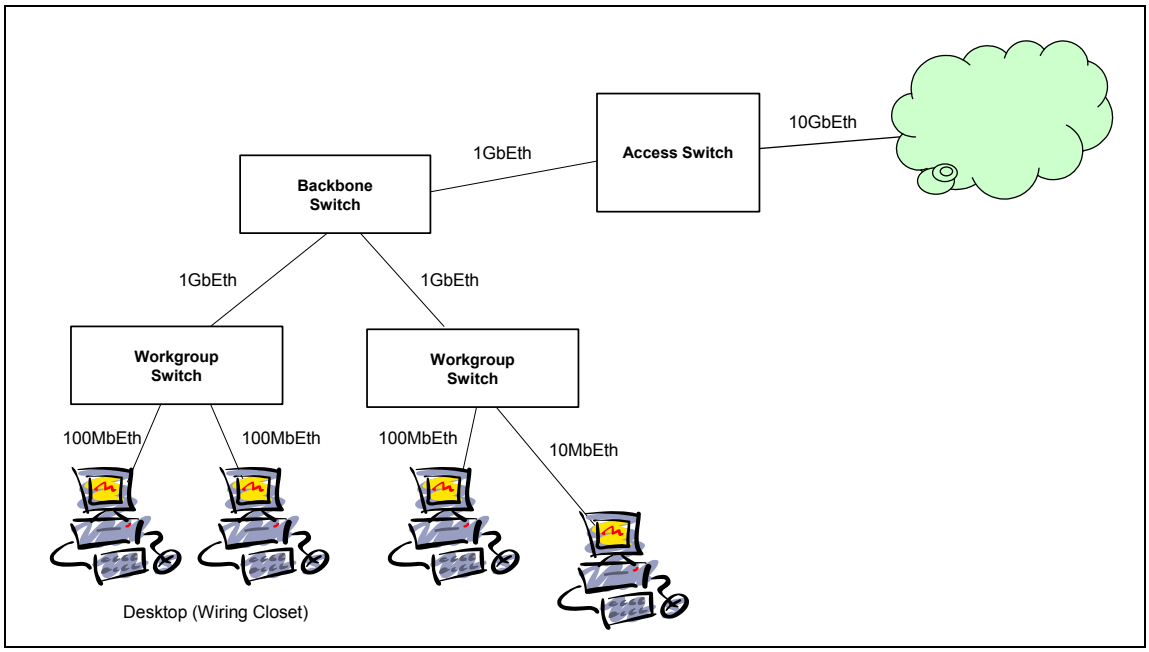

Figure 1: Enterprise LAN Topology Example

The programmable 10/100/100/10000 AnySpeed Ethernet MAC from MorethanIP provides, with a single IP Core, a solution for Ethernet applications (Line Card, NIC card or switching) operating at 10/100/1000Mbps (Gigabit Ethernet) or 10000Mbps (10 Gigabit).

The AnySpeed MAC, together with MorethanIP 1000 / 2500Base-X PCS Core can also be used to implement proprietary or industry standard 2.5Gpbs Ethernet links.

The AnySpeed MAC Core operates Full Duplex mode, supports transparent (For switching applications) and Ethernet frame termination / generation (For NIC or line cards applications) with padding and wire speed CRC check / generation.

The core can seamlessly connect to any industry standard Ethernet PHY devices via an extended 16-Bit Gigabit Medium Independent Interface for Gigabit and 2.5 Gigabit Ethernet applications and a XGMII interface for 10 Gigabit Ethernet applications.

On the Client interface, the Core implements a 64-Bit SOC (System on a Chip) interface which provides seamless connectivity to any MorethanIP cores or third party Cores, such as PCI-Express interfaces, which implements an interface compatible with the Altera Atlantic specification.

2 Application Example

The Example on “Figure 2” shows how the Converter is used to implement, with other MorethanIP IP Cores (10GBase-KX4, 1000 / 2500Base-KX PCS Cores and Autonegotiation), a complete Ethernet Backplane Transceiver compliant with IEEE802.3ap standard and support industry standard 2.5Gbps Backplane connections.

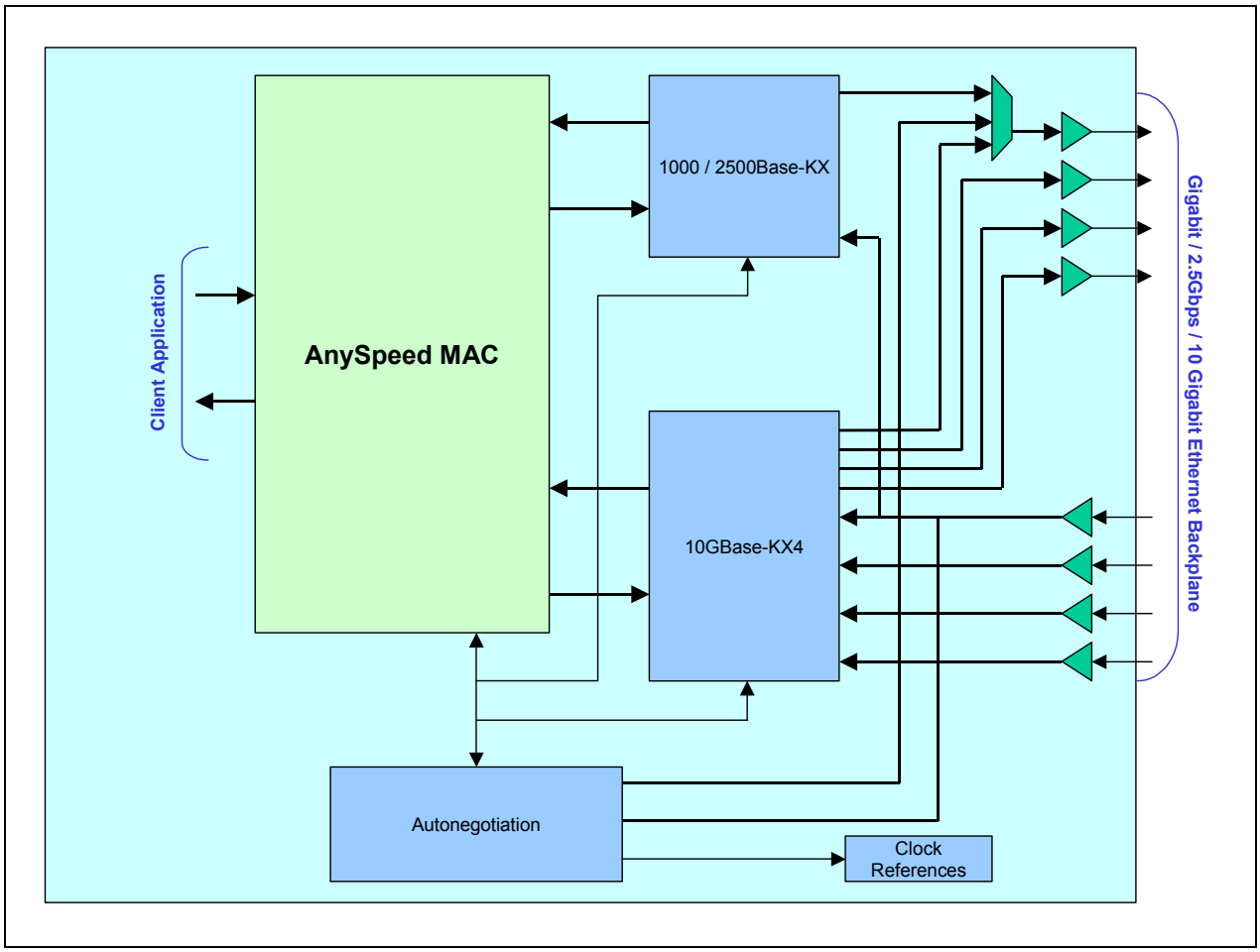

Figure 2: Application Example – 10 Gigabit / Gigabit / 2.5GbpsEthernet Backplane

3 AnySpeed Ethernet MAC Core Features Overview

- Full MAC layer and Reconciliation sub-layer implementation compliant with IEEE802.3ae specification
- Dynamically configurable to support 10 Gigabit Ethernet, with XGMII interface, or Gigabit with GMII interface, applications
- Can be configured for NIC (Network Interface Card) applications or Switching / Bridging applications
- Lane, data alignment, PHY error and local/remote fault signaling handled by the Core's Reconciliation sub-layer
- CRC-32 checking at full speed using a multi-stage CRC calculation architecture with optional forwarding of the FCS field to the user application
- CRC-32 generation and append on transmit or forwarding of user application provided FCS selectable on a per-frame basis
- Optional MAC address comparison on receive and overwrite on transmit for NIC applications
- Selectable promiscuous frame receive mode and transparent MAC address forwarding on transmit
- Optional Multicast address filtering with 64-bin hash code lookup table on receive reducing processing load on higher layers
- Optional Ethernet Pause Frame (802.3 Annex 31A) termination providing fully automated flow control without any user application overhead
- Optional automatic Pause Frame generation from programmable FIFO congestion thresholds or by dedicated command pin with programmable Quanta
- Programmable frame maximum length providing support for any frame (e.g. Jumbo Frame or any tagged Frame)
- Support for VLAN tagged frames according to IEEE 802.1Q specification in both transmit and receive
- Dynamic inter packet gap (IPG) calculation for WAN applications
- Deficit Idle Counter (DIC) for optimized performance with minimum IPG for LAN applications
- Clock and data rate decoupling with programmable asynchronous FIFOs
- 64-Bit User application interface compatible with Altera Atlantic SOC (System On-Chip) interface
- Optional 802.3 basic and mandatory managed Objects statistic counters and IETF Management Information Database (MIB) package (RFC2665) and Remote Network Monitoring (RMON) counters

10 AnySpeed MAC Controller Core Block Diagram

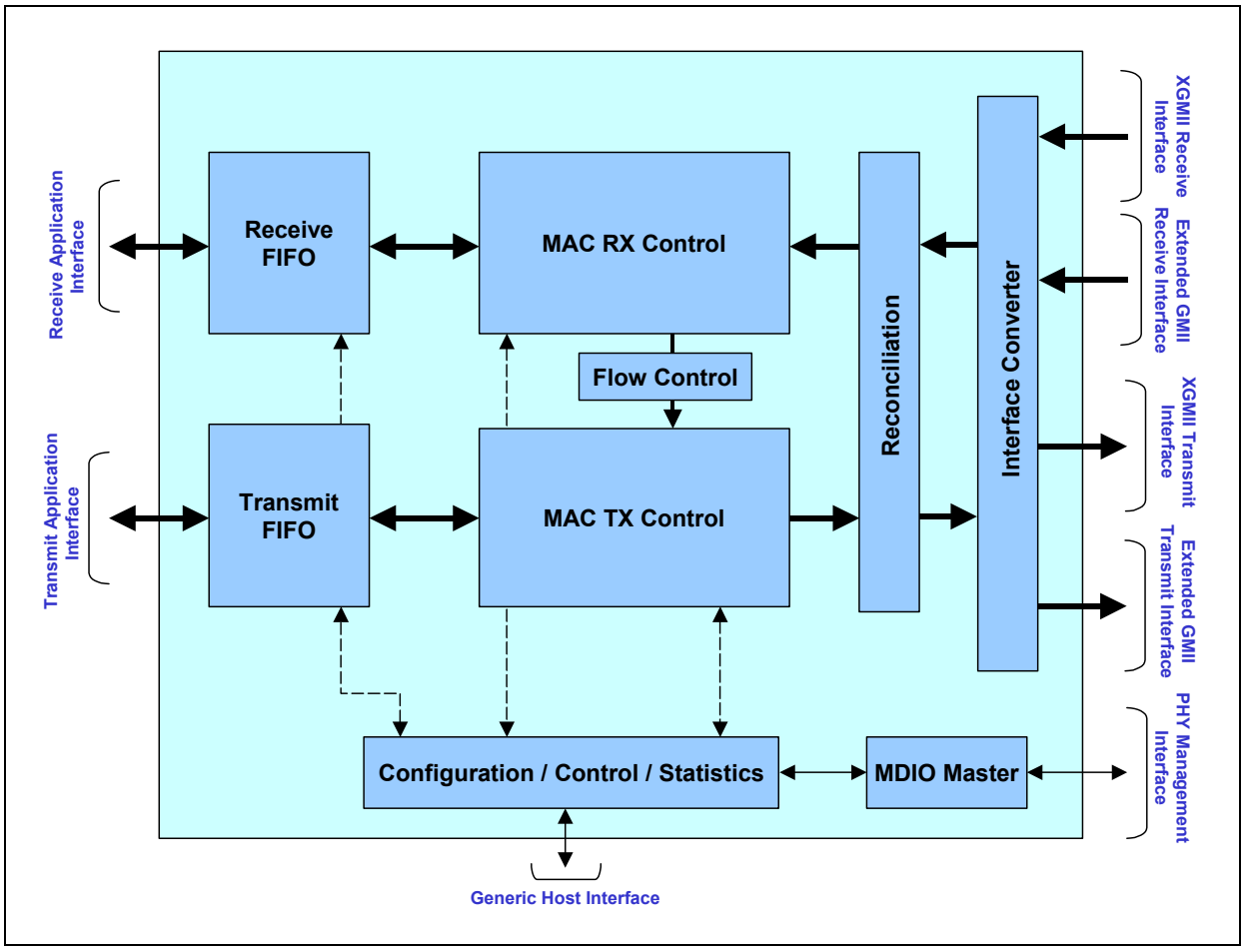

Figure 3: AnySpeed MAC Controller Core Block Diagram

4 Implementation Summary

Table 1: Altera FPGA Implementation Summary

Target Device Family	Speed Grade	Complexity (With 256x64 FIFOs)	Performance	Requirement
Stratix-II	C5	6000 to 7900 LEs (1)	190MHz	156.25MHz

1. The Logic Element count for Stratix II devices is based on the number of adaptive look-up tables (ALUTs) used for the design as reported by the Quartus II software.

Table 2: Altera Structured ASIC Implementation Summary

Target Device Family	Complexity (With 256x64 FIFOs)	Performance	Requirement
Hardcopy-II	24000 to 33000 HCells	210Mhz	156.25MHz

5 Design Package and Support

Table 3: Design Kit Overview

Design and Simulation	
Language	VHDL / Verilog Source Code or Encrypted VHDL / Verilog Sources Code for Altera FPGAs.
Simulation	Configurable VHDL / Verilog Testbench with embedded frame generator and checker providing an easy to use and robust de-bugging environment.
Verification	Comprehensive test environment with Ethernet frame generator and verification models for standard compliant and errored frame generation and automated core behavior verification.
Supported Design Tools	
Simulation	Modelsim Version 5.7a or higher.
Synthesis	Altera: Quartus II V5.0 or Higher
Implementation	Altera: Quartus II V5.0 or Higher

6 Ordering Information

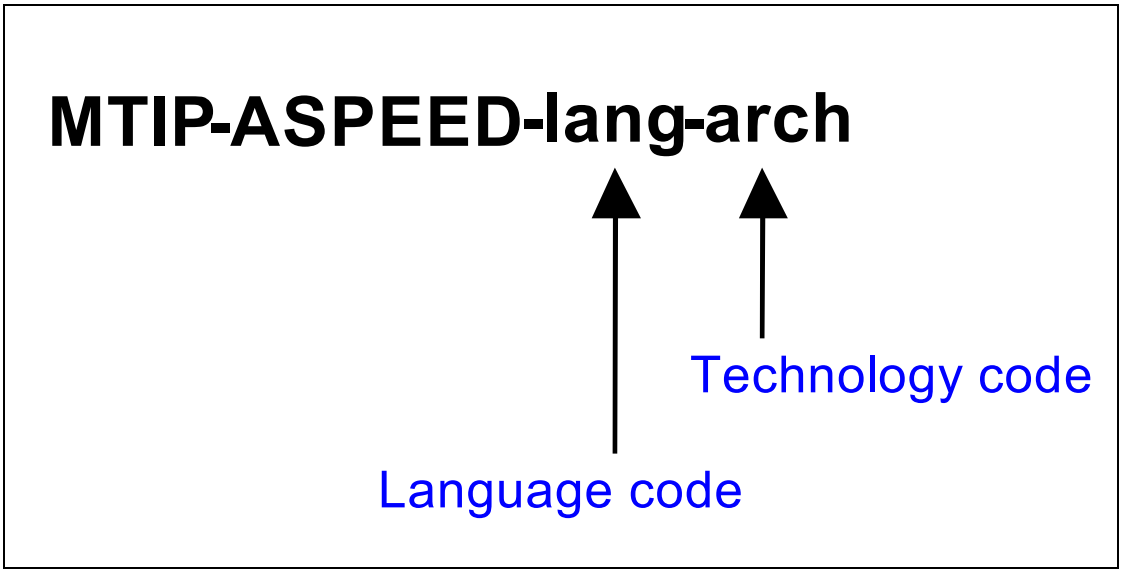

Table 4: Language Code

Language Code	*Delivery Language*
BIN	Encrypted VHDL / Verilog Sources Code for Altera FPGAs and Structured ASICs.
VHDL	Synthesizable generic VHDL source code for Altera FPGA and Structured ASICs or ASIC implementations
VLOG	Synthesizable generic Verilog source code for Altera FPGA and Structured ASICs or ASIC implementations

Table 5: Technology Code

Technology Code	*Target Technology*
GEN	Source code option for Altera FPGAs (STRATIX-II or STRATIX GX) and Structured ASICs.or Hardcopy Structured ASIC.
ALTR	Encrypted netlist for Altera FPGAs (STRATIX-II or STRATIX GX) and Hardcopy Structured ASICs.

7 Contact

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