SPAUI MAC Core Product Brief

Version 1.1 - May 2008

Introduction

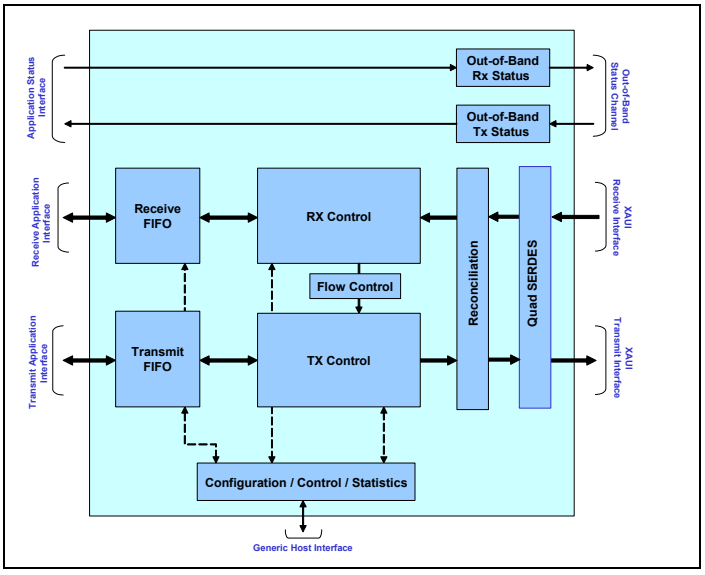
The SPAUI Protocol provides a proprietary open mechanism, originally from Dune Networks, to interconnect MAC/Framer, Network Processor, and Traffic Manager. SPAUI combines the benefits of both XAUI and SPI4.2 to support additional services such as per channel flow control segmentation and burst traffic.

The SPAUI MAC Core implements, on the Client side, a flexible simple 64-Bit FIFO interface designed to be seamlessly connected to standard Core (e.g. SPI-4) or customer applications. The SPAUI MAC can be field configured to operate in standard IEEE802.3ae mode or to implement the SPAUI extended services.

On the Ethernet Line side, the Core can be configured to implement either a XAUI (10 Gigabit Attachment Unit Interface) when the design is targeted to low cost Arria GX, feature rich Stratix II GX or Stratix IV FPGA.

Optionally, the Core can be connected to MorethanIP 2-Lane RXAUI (Reduced XAUI) Core to increase the port density.

The SPAUI Core can be used in a single FPGA or ASIC device, for example, to implement a Bridging function between a Network Processor and Traffic Manager.



SPAUI MAC Core Block Diagram

SPAUI MAC Core Features Overview

- Full MAC layer and Reconciliation sub-layer implementation compliant with IEEE802.3ae specification with SPAUI functions extension
- Standard preamble and SFD insertion and deletion with optional insertion of a user specific 8-Byte preamble with support for BCT (Burst Control Tag) Bytes
- Lane, data alignment, PHY error and local/remote fault signaling handled by the Core's Reconciliation sub-layer
- CRC-32 checking at full speed using a multi-stage CRC calculation architecture
- BCT Bytes CRC-4 generation and checking
- Burst and segmented frames supported with BCT bytes
- Optional MAC address comparison on receive and overwrite on transmit for NIC applications
- Selectable promiscuous frame receive mode and transparent MAC address forwarding on transmit
- Supports standard Ethernet Pause Frame (802.3 Annex 31A) termination and generation with programmable Quanta
- Supports for SPAUI in-band extended class based flow control frames, Link Level Flow Control (LLFC) with BCT Bytes and packet agnostic pause frame format
- Implements Out-of-Band status interface with programmable calendar and synchronization parameters
- Programmable frame maximum length providing support for any frame (e.g. Jumbo Frame or any tagged Frame)
- Support for VLAN tagged frames according to IEEE 802.1Q specification in both transmit and receive
- Deficit Idle Counter (DIC) for optimized performance with minimum IPG for LAN applications and SPAUI IPG compression
- Clock and data rate decoupling with programmable asynchronous FIFOs
- Optional Padding termination/insertion for NIC applications or forwarding of unmodified frames for switching applications
- Implements statistics and event for IEEE802.3 basic and mandatory managed Objects and IETF Management Information Database (MIB) package (RFC2665) and Remote Network Monitoring (RMON) required in SNMP environments

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Implementation Summary

Arria GX Implementation Summary

	Min	Max
Speed Grade	C6	
LEs	4400	9000
RAM Blocks	13	Setting dependent
Serdes Channels	4	4

Stratix II GX Implementation Summary

	Min	Max
Speed Grade	C5	
LEs	4400	9000
RAM Blocks	13	Setting dependent
Serdes Channels	4	4

Stratix IV Implementation Summary

	Without Rate Matching	With Rate Matching
Speed Grade	C4	
LEs	4160	8900
RAM Blocks	13	Setting dependent
Serdes Channels	4	4

The Logic Element count for Stratix II devices is based on the number of adaptive look-up tables (ALUTs) used for the design as reported by the Quartus II software.

Deliverables

- Verilog or VHDL Synthesizable RTL HDL or encrypted RTL for FPGA implementation
- Behavioral Verilog or VHDL testbenches and Verification test cases
- One year of technical support by MorethanIP development team

Supported Tools

Supported FPGA Design Tools

Implementation	Altera Quartus II 8.0 or later
Simulation	Modelsim 5.7d or Later
Synthesis	Altera Quartus II 8.0 or later

Ordering Code

MTIP-SPAUIM-lang-tech

technology code

language code

Language Code	*Delivery Language*
VHDL	Synthesizable RTL VHDL Source Code.
VLOG	Synthesizable RTL Verilog Source Code.
BIN	Encrypted RTL for Altera FPGA technology.

Technology Code	*Target Technology*
GEN	Generic sythesizable code for ASIC or FPGA implementations
ALTR	Synthesizable code optimized Altera FPGAs.

Contact

MorethanIP

E-Mail : info@morethanip.com

Internet : www.morethanip.com

Muenchner Strasse 199

D-85757 Karlsfeld

Germany

Tel : +49 (0) 8131 333939 0

FAX : +49 (0) 8131 333939 1