SPAUI MAC Core Product Brief

Version 1.1 - May 2008

Introduction

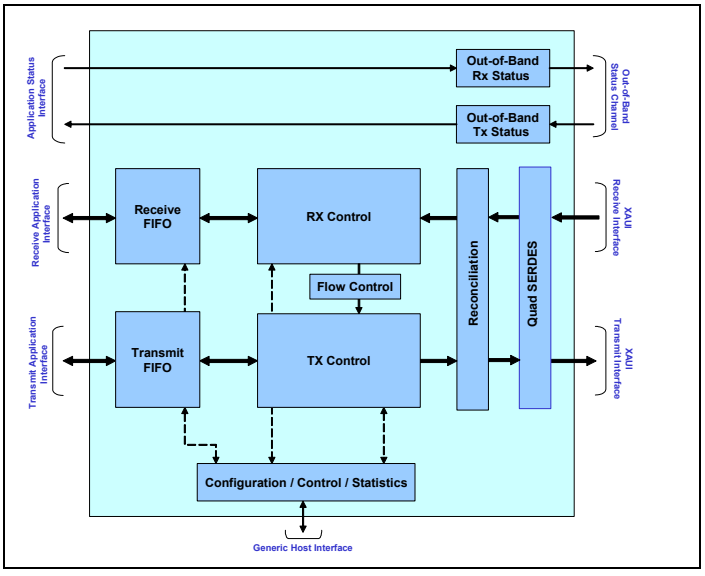
The SPAUI Protocol provides a proprietary open mechanism, originally from Dune Networks, to interconnect MAC/Framer, Network Processor, and Traffic Manager. SPAUI combines the benefits of both XAUI and SPI4.2 to support additional services such as per channel flow control segmentation and burst traffic.

The SPAUI MAC Core implements, on the Client side, a flexible simple 64-Bit FIFO interface designed to be seamlessly connected to standard Core (e.g. SPI-4) or customer applications. The SPAUI MAC can be field configured to operate in standard IEEE802.3ae mode or to implement the SPAUI extended services.

On the Line side, the Core implements a XAUI (10 Gigabit Attachment Unit Interface) when the design is targeted to Xilinx Virtex 5 LXT or FXT FPGAs.

Optionally, the Core can be connected to MorethanIP 2-Lane RXAUI (Reduced XAUI) Core to increase the port density.

The SPAUI Core can be used in a single FPGA or ASIC device, for example, to implement a Bridging function between a Network Processor and Traffic Manager.



SPAUI MAC Core Block Diagram

SPAUI MAC Core Features Overview

- Full MAC layer and Reconciliation sub-layer implementation compliant with IEEE802.3ae specification with SPAUI functions extension
- Standard preamble and SFD insertion and deletion with optional insertion of a user specific 8-Byte preamble with support for BCT (Burst Control Tag) Bytes
- Lane, data alignment, PHY error and local/remote fault signaling handled by the Core's Reconciliation sub-layer
- CRC-32 checking at full speed using a multi-stage CRC calculation architecture
- BCT Bytes CRC-4 generation and checking
- Burst and segmented frames supported with BCT bytes
- Optional MAC address comparison on receive and overwrite on transmit for NIC applications
- Selectable promiscuous frame receive mode and transparent MAC address forwarding on transmit
- Supports standard Ethernet Pause Frame (802.3 Annex 31A) termination and generation with programmable Quanta
- Supports for SPAUI in-band extended class based flow control frames, Link Level Flow Control (LLFC) with BCT Bytes and packet agnostic pause frame format
- Implements Out-of-Band status interface with programmable calendar and synchronization parameters
- Programmable frame maximum length providing support for any frame (e.g. Jumbo Frame or any tagged Frame)
- Support for VLAN tagged frames according to IEEE 802.1Q specification in both transmit and receive
- Deficit Idle Counter (DIC) for optimized performance with minimum IPG for LAN applications and SPAUI IPG compression
- Clock and data rate decoupling with programmable asynchronous FIFOs
- Optional Padding termination/insertion for NIC applications or forwarding of unmodified frames for switching applications
- Implements statistics and event for IEEE802.3 basic and mandatory managed Objects and IETF Management Information Database (MIB) package (RFC2665) and Remote Network Monitoring (RMON) required in SNMP environments

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Implementation Summary

Xilinx FPGA Implementation Summary

Core Specifics		
Supported Device Family	Virtex-5 LXT / FXT	
Version	1.1	
Resources Used		
	Min	**Max**
LUTs	3,746	7,815
FFs	4,293	8,884
Block RAM	10	User Setting Dependent
GTPs	2	2
DCMs	Virtex 5 LXT: 1 Virtex 5 FXT: 0	Virtex 5 LXT: 1 Virtex 5 FXT: 0
Provided with Core		
Documentation	Datasheet, User Guide	
Design File Formats	Source RTL VHDL or Verilog Encrypted RTL VHDL or Verilog	
Constraints File	UCF File	
Verification	VHDL or Verilog Self-Checking Testbench	
Supported Design Tools		
Xilinx Tool	10.1i or Later	
Simulation	Modelsim 6.2 or Later	
Synthesis	XST	
Required Speed Grade		
3.125Gbps Serdes	Virtex-5 LXT: -1 Virtex-5 FXT: -1	
3.75Gbps Serdes	Virtex-5 LXT: -2 Virtex-5 FXT: -1	Virtex-5 LXT: -2 Virtex-5 FXT: -1
Up to 6.5Gbps Serdes	Virtex-5 FXT: -1 or -2	

Ordering Code

MTIP-SPAUIM-lang-tech

technology code

language code

Language Code	*Delivery Language*
VHDL	Synthesizable RTL VHDL Source Code.
VLOG	Synthesizable RTL Verilog Source Code.
BIN	Encrypted RTL for Xilinx FPGA technology.

Technology Code	*Target Technology*
GEN	Generic sythesizable code for ASIC or FPGA implementations
XLNX	Synthesizable code optimized Xilinx FPGAs.

Contact

MorethanIP

E-Mail : info@morethanip.com

Internet : www.morethanip.com

Muenchner Strasse 199

D-85757 Karlsfeld

Germany

Tel : +49 (0) 8131 333939 0

FAX : +49 (0) 8131 333939 1

UNH Member