10 Gigabit Reduced XAUI PCS Core Product Brief

Version 1.0 - June 2008

Introduction

The RXAUI (10 Gigabit Reduced Attachment Unit Interface) interface provides a low pin count board level interface to connect a 10 Gigabit Ethernet MAC to a physical device or for backplane connectivity.

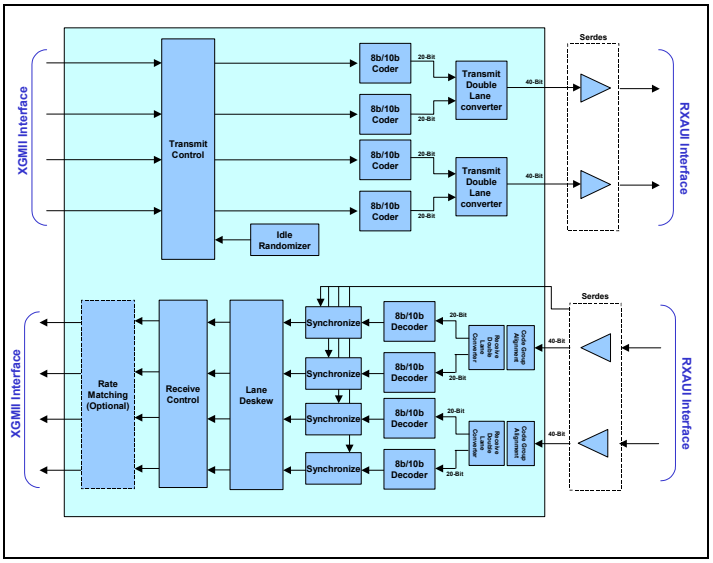
The RXAUI PCS Core implements a XGXS (10 Gigabit Extension Sub-Layer) PCS function (Physical Coding Sub-Layer) Core, designed to comply with the IEEE802.3ae Clause 48 and can be used, with four to two multiplexing and two to four lane demultiplexing functions.

The RXAUI Core provides a low pin count board level interface to PHY devices or for backplane applications. The Core is also compliant for Dune Network Dual Rate PHY interface.

On the MAC or application side, the RXAUI PCS Core implements a 64-Bit de-multiplexed XGMII interface or a standard 32-Bit DDR (Dual Data Rate).

On the line side can be used in combination with an embedded Dual 6.25Gbps SERDES or, via a dual 20-Bit interface, with an external SERDES.

The Core can be used with Altera Stratix II GX and Stratix IV parts to increase per device port density and improve board level design.



10 Gigabit RXAUI Core Block Diagram

RXAUI PCS Core Features Overview

- Implements a XGXS PCS function fully compliant with the IEEE802.3ae Clause 48 specification
- Core XGXS functions passed complete UNH certification
- Implements XGXS PCS frame encapsulation / de-encapsulation with Start, Terminate ordered set insertion / termination and Randomized Idle ordered set generation during inter-packet gap
- Implements receive link synchronization state machine and 10-Bit data alignment from SERDES with Comma character detection
- Link coding implemented with 8B/10B providing DC balanced bitstream for efficient SERDES operation
- Dual 20-Bit interface to embedded or external 6.25Gbps SERDES
- Implements a 64-Bit XGMII interfaces that can be seamlessly connected to MorethanIP 10 Gigabit Ethernet MAC Core or to any other third party MAC Core
- Optional rate matching to adapt Rates from the RXAUI Line clock with the XGMII Receive Clock
- Link coding implemented with 8B/10B providing DC balanced bitstream for efficient SERDES operation
- Implements a link synchronization state machine per port
- Receive Lane alignment (Deskew) designed to compensate RXAUI lines skew
- Line alignment exceeds IEEE802 lane skew tolerance requirements
- Optional Rate matching Function
- The RXAUI Core can be implemented in Altera Stratix II GX and Stratix IV FPGAs, Structured ASICs or ASICs.
- The Core is optionally be delivered in Verilog source code or encrypted Verilog code which provides a lower cost licensing option

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Implementation Summary

Stratix II GX Implementation Summary

	Without Rate Matching	With Rate Matching
Speed Grade	C5	
LEs	2700	3200
RAM Blocks	4 M512s	4 M512s + 2 M4Ks
Serdes Channels	2	2

Stratix IV Implementation Summary

	Without Rate Matching	With Rate Matching
Speed Grade	C4	
LEs	2550	3200
RAM Blocks	4 M9Ks	6 M9Ks
Serdes Channels	2	2

The Logic Element count for Stratix II devices is based on the number of adaptive look-up tables (ALUTs) used for the design as reported by the Quartus II software.

Deliverables

- Verilog Synthesizable RTL HDL or encrypted RTL for FPGA implementation
- Behavioral Verilog testbenches and Verification test cases
- One year of technical support by MorethanIP development team

Supported Tools

Supported FPGA Design Tools

Implementation	Altera Quartus II 8.0 or later
Simulation	Modelsim 5.7d or Later
Synthesis	Altera Quartus II 8.0 or later

Ordering Code

MTIP-RXAUI-lang-tech

technology code

language code

Language Code	*Delivery Language*
VLOG	Synthesizable RTL Verilog Source Code.
BIN	Encrypted RTL for Altera FPGA technology.

Technology Code	*Target Technology*
GEN	Generic synthesizable code for ASIC or FPGA implementations
ALTR	Synthesizable code optimized Altera FPGAs.

Contact

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