Product Brief
Version 3.5 - August 2004

1 Introduction

Ethernet is available in different speeds (10 and 100Mbps) and provides connectivity to meet a wide range of needs and from desktop to switches. MorethanIP IP solutions provide a solution for each Ethernet application with a library of configurable MAC (Medium Access Control) and PCS (Physical Coding Sub-layer) Cores.

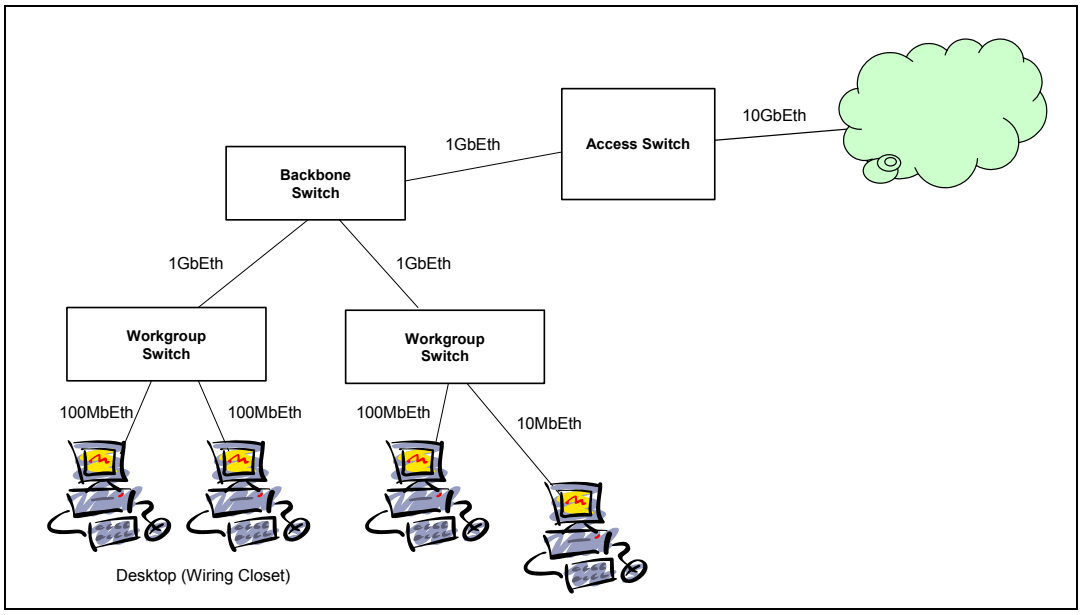

Figure 1: Enterprise LAN Topology Example

The programmable 10/100 Ethernet MAC from MorethanIP provides, with a single IP Core solution, a solution for Ethernet applications (Line Card, NIC card or switching) operating at 10 or 100Mbps (Fast Ethernet). The 10/100 MAC Core can operate in Half Duplex or Full Duplex mode, supports transparent (For switching applications) and full Ethernet frame termination / generation (For NIC or line cards applications).

The core can be seamlessly connected to any industry standard Medium Independent Interface and to a user application via a SOC (System on a Chip) interface which provides seamless connectivity to any MorethanIP cores such as Flexbus, POS-PHY, PCI interfaces or any third party Core which implements an interface compatible with the Altera Atlantic specification.

The core is optionally delivered in generic synthesizable HDL code (For use in FPGA or ASIC technologies), as a FPGA netlist.

2 Application Example

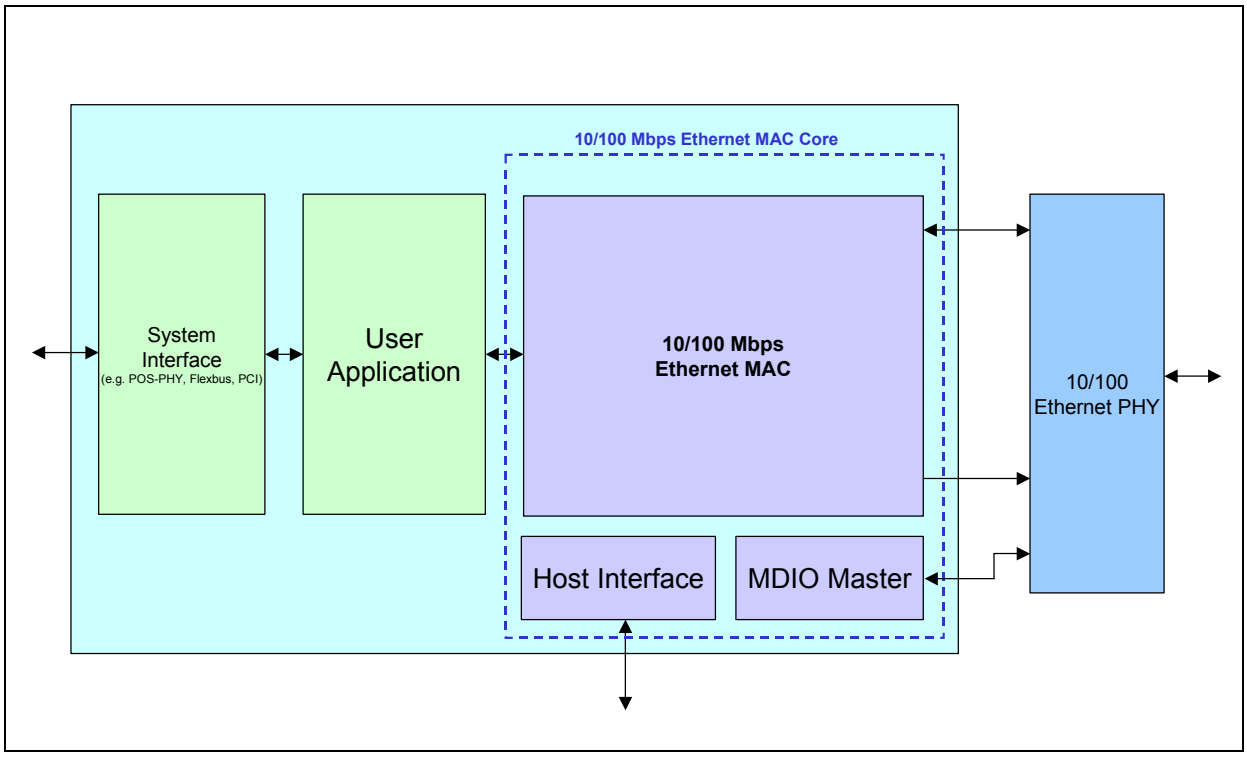

Figure 2: Application Example

3 10/100Mbps Ethernet MAC core Features

- Implements the full 802.3 specification with preamble / SFD generation, frame padding generation, CRC generation and checking on transmit and receive respectively
- Dynamically configurable to support 10Mbps or 100Mbps operation
- Supports Full Duplex or Half Duplex operation selectable via a Core configuration option
- Supports AMD Magic Packet detection for node remote power management
- Seamless interface to commercial Fast Ethernet PHY device via a 4-Bit Medium Independent Interface (MII) operating at 25MHz
- Simple FIFO interface to user application compatible with Altera Atlantic SOC (System On Chip) interface
- CRC-32 checking at full speed using a multi-stage CRC calculation architecture with optional forwarding of the FCS field to the user application
- CRC-32 generation and append on transmit or forwarding of user application provided FCS selectable on a per-frame basis
- When operating in Full Duplex mode, implements fully automated Pause Frame (802.3 Annex 31A) generation and termination providing flow control without user application intervention
- When operating in full duplex mode, pause quanta used to form Pause frames, dynamically programmable
- Pause frame generation additionally controllable by user application offering flexible traffic flow control

- Optional forwarding of received pause frames to the user application when operating in Full Duplex mode
- Implements standard flow-control mechanism in full-duplex operation mode
- In half-duplex mode, provides full collision support, including jamming, backoff, and automatic retransmission
- Support for VLAN tagged frames according to IEEE 802.1Q
- Programmable MAC address: Insertion on transmit; discards frames with mismatching destination address on receive (except broadcast and pause frames)
- Programmable group of four supplemental MAC addresses that can be used to accept / reject Unicast traffic
- Programmable Promiscuous mode support to omit MAC destination address checking on receive
- Multicast address filtering on receive based on 64 entries hash table reducing higher layer processing load
- Programmable frame maximum length providing support for any standard or proprietary frame length (e.g. 9K-Bytes Jumbo Frames)
- Optional internal MII Loopback
- Statistics indicators for frame traffic as well as errors (alignment, CRC, length) and pause frames providing for IEEE 802.3 basic and mandatory Management Information Database (MIB) package as well as Ethernet MIB (RFC 2665) and Remote Network Monitoring (RFC 2819) enabling implementation in SNMP management environments
- Simple handshake user application FIFO interface with fully programmable depth and threshold levels ensuring data rates of 1Gbps with full back-to-back frame transfer support
- 8-Bit or 32-Bit Client FIFO interface
- Separate status word available for each received frame on the user interface providing information such as frame length, frame type, VLAN tag and error information
- MDIO Master interface for PHY device configuration and management with two programmable MDIO base addresses
- Available for FPGA or ASIC implementation
- Design Kit comes with extensive Ethernet frame generators and checking models enabling fully automated design verification and testing for standard compliance and error behavior, enabling for fast turn-around design cycles

4 MAC Core Block Diagram

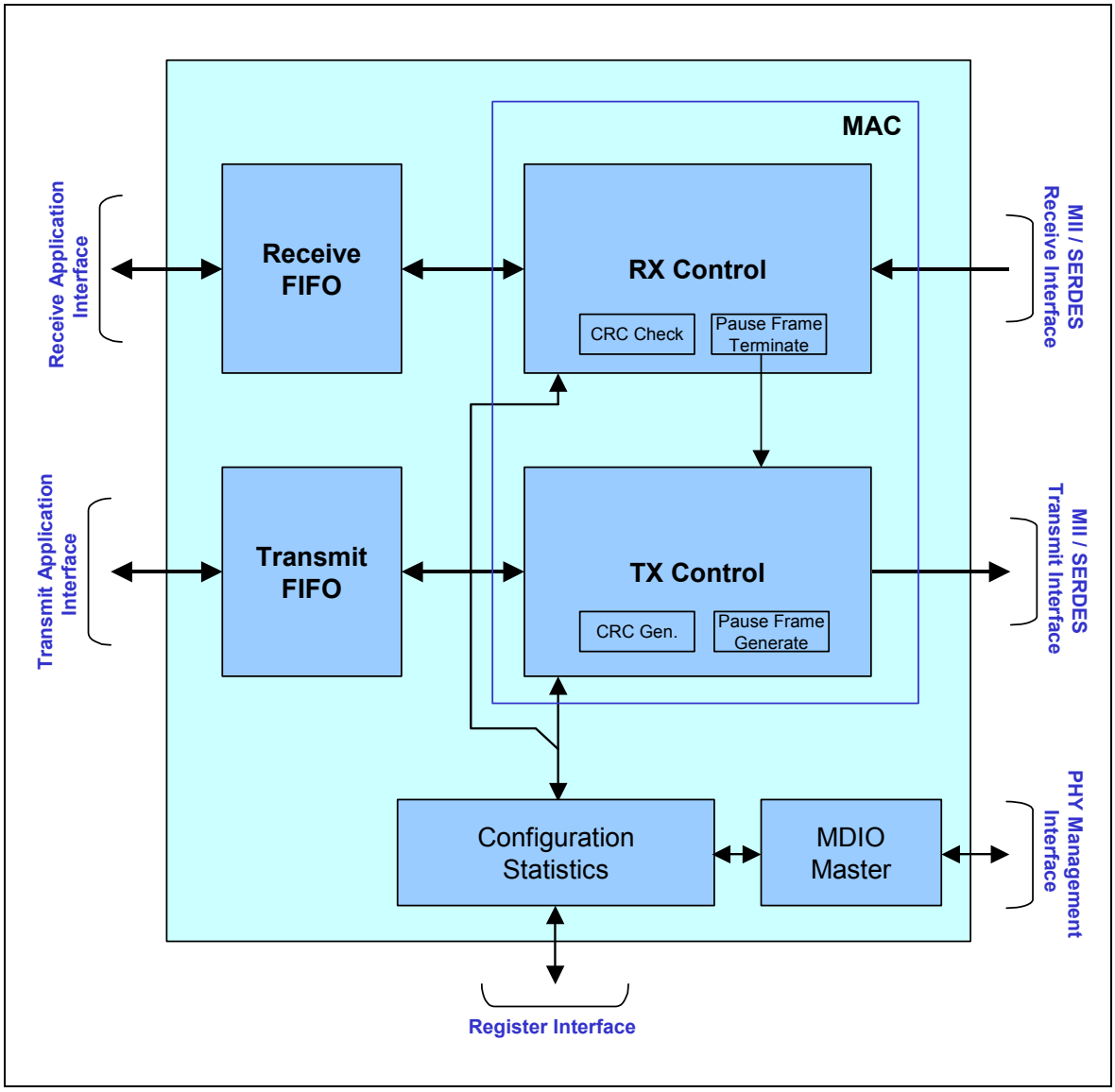

Figure 3: 10/100Mbps Ethernet MAC Core Overview

5 Implementation Summary

5.1 10/100 Mbps MAC Core with Statistic Registers and MDIO Master

Table 1: 10/100 Ethernet MAC with Statistics Registers and MDIO Master complexity Summary

Target Device Family	**Speed Grade**	**Complexity** (With 256 Bytes FIFOs)	**Performance**	**Requirement** (Fast Ethernet)
STRATIX II	-5	3500 ALUTs	150MHz	25MHz
CYCLONE II	-8	3600 LEs	120MHz	25MHz
STRATIX	-8	3600 LEs	100MHz	25MHz
CYCLONE	-8	3600 LEs	100MHz	25MHz

5.2 10/100Mbps MAC Core without Statistics and Register Map

Table 2: 10/100 Ethernet MAC without Statistics and Register Interface, Complexity Summary

Target Device Family	**Speed Grade**	**Complexity** (With 256 Bytes FIFOs) LEs	**Performance**	**Requirement** (Fast Ethernet)
STRATIX II	-5	1850 ALUTs	150MHz	25MHz
CYCLONE II	-8	1900 LEs	120MHz	25MHz
STRATIX	-8	1900 LEs	100MHz	25MHz
CYCLONE	-8	1900 LEs	100MHz	25MHz

6 10/100Mbps Ethernet MAC Design Kit Overview

Table 3: Design Kit Overview

Design and Simulation	
Language	Optimized VHDL / Verilog or cost effective FPGA encrypted netlist.
Simulation	Configurable VHDL / Verilog Testbench with embedded frame generator and checker providing an easy to use and robust de-bugging environment.
Verification	Comprehensive test environment with Ethernet frame generator and verification models for standard compliant and errored frame generation and automated core behavior verification.
Supported Design Tools	
Simulation	Modelsim Version 5.7a or higher.
Synthesis	Exemplar Leonado 2003a or higher Exemplar Precision 2003c or higher Synplicity Synplify 7.3 or Higher
Implementation	Quartus II 3.0 or higher

7 References

1. IEEE 802.3 2002 Edition
2. IEEE 802.1Q 1998 Edition
3. RFC2665, Definitions of Managed Objects for the Ethernet-like Interface Type, www.ietf.org
4. RFC2863, The interfaces Group MIB, www.ietf.org

8 Ordering Code

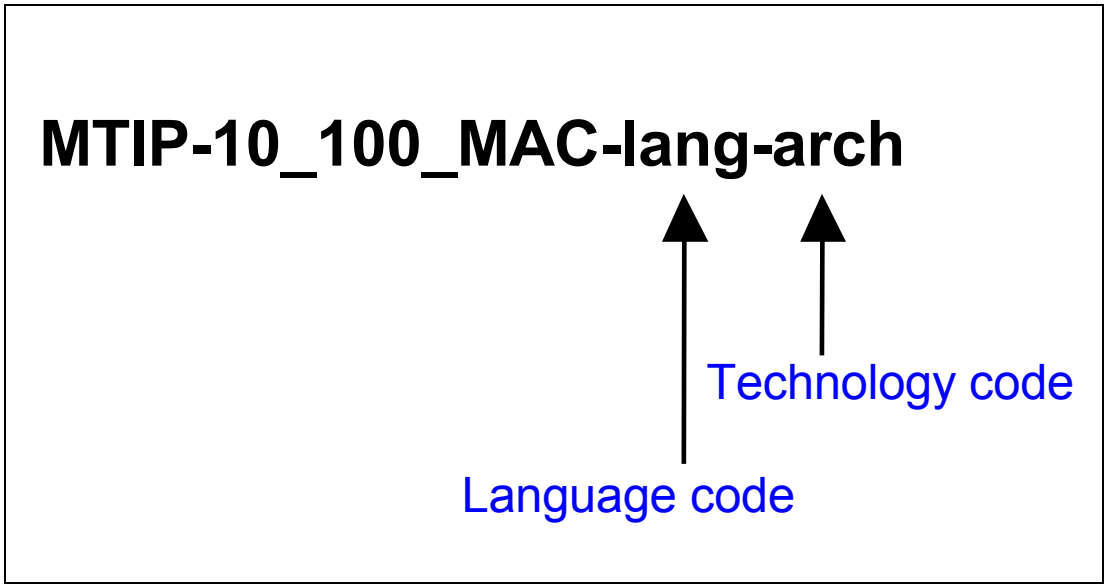

Table 4: Language Code

Technology Code	Target Technology
BIN	Encrypted FPGA netlist.
VHDL	Synthesizable generic VHDL source code for FPGA or ASIC implementations
VLOG	Synthesizable generic Verilog source code for FPGA or ASIC implementations

Table 5: Technology Code

Technology Code	Target Technology
GEN	VHDL or Verilog Source code option.
ALTR	Encrypted Netlist for Altera FPGAs.

9 Contact

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