10/100/1000Mbps Ethernet MAC Core

Version 3.65 - September 2007

Introduction

Ethernet is available in different speeds (10/100/1000 and 10000Mbps) and provides connectivity to meet a wide range of needs from desktop to switches. MorethanIP IP solutions provide a solution for each Ethernet application with a library of configurable MAC (Media Access Control) and PCS (Physical Coding Sub-layer) Cores.

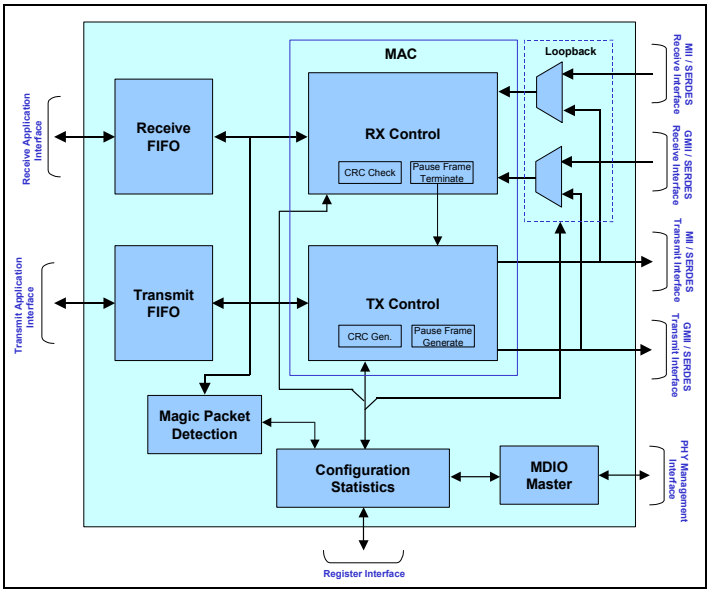
The programmable 10/100/100 Ethernet MAC from MorethanIP provides, with a single IP Core, a solution for Ethernet applications (Line Card, NIC card or switching) operating at 10/100 or 1000Mbps (Gigabit Ethernet). The 10/100/1000 MAC Core operates Full Duplex mode, supports transparent (For switching applications) and full Ethernet frame termination / generation (For NIC or line cards applications).

For efficient power management, the Core also implements Magic Packets detection.

The core can seamlessly connect to any industry standard Gigabit Ethernet PHY device via a Gigabit Medium Independent Interface (GMII for 1000Mbps application) or Medium Independent Interface (MII for 10/100Mbps applications) and to a user application via a SOC (System on a Chip) interface, which provides seamless connectivity to any MorethanIP cores such, or third party Core.

MorethanIP can also provide 1000Base-X PCS (Physical Coding Sublayer) Core and SGMII, RMII, RGMII, SSSMII modules to implements low pin count interfaces.

The Core is fully UNH certified and is interoperable with major PHY vendor and systems.



10/100/1000Mbps Ethernet MAC Core Overview

10/100/1000Mbps Ethernet MAC core Features

- Implements the full 802.3 specification with preamble / SFD generation, frame padding generation, CRC generation and checking on transmit and receive respectively
- Dynamically configurable to support 10Mbps, 100Mbps or 1Gbps operation
- Supports AMD Magic Packet detection for node remote power management
- Supports, for 10/100Mbps operation, full duplex or half duplex operation selectable via a Core configuration option
- Simple 8 or 32-Bit FIFO interface to Client application
- Implements fully automated XON and XOFF Pause Frame (802.3 Annex 31A) generation and termination
- Pause frame generation controllable by user application offering flexible traffic flow control
- In half-duplex mode, provides full collision support, including jamming, backoff, and automatic retransmission
- Support for VLAN tagged frames according to IEEE 802.1Q
- Programmable MAC address: Insertion on transmit; discards frames with mismatching destination address on receive (Except Broadcast and frames)
- Programmable group of four supplemental MAC addresses that can be used to accept / reject Unicast traffic
- Programmable Promiscuous mode support to omit MAC destination address checking on receive
- Multicast address filtering on receive based on 64 entries hash table reducing higher layer processing load
- Programmable frame maximum length providing support for any standard or proprietary frame length (e.g. 9K-Bytes Jumbo Frames)
- Optional internal GMII / MII Loopback
- Optional automatic receive errored frame discard
- Separate status word available for each received frame on the user interface providing information such as frame length, frame type, VLAN tag and error information
- MDIO Master interface for PHY device configuration and management with two programmable MDIO base addresses
- Optional statistics 32-Bit counters for IEEE 802.3 basic and mandatory Management Information Database (MIB) package as well as Ethernet MIB (RFC 2665) and Remote Network Monitoring (RFC 2819)

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Implementation Summary

Altera FPGA Implementation Summary

Target Device Family	Speed Grade	Complexity	Performance
Stratix III	C4L	2,400 to 4,000 LEs (1)	165MHz
	C4		220MHz
Cyclone III	C8	2,550 to 4,400 LEs	160MHz
Arria GX	C6	2,200 to 3,350 LEs (1)	170MHz
Stratix II	C5	2,200 to 3,350 LEs (1)	200MHz
Stratix II GX	C5	2,200 to 3,350 LEs (1)	200MHz
Cyclone II	C8	2,500 to 4.350 LEs	135MHz

1. The Logic Element count for Stratix II , Stratix III, Arria GX devices is based on the number of adaptive look-up tables (ALUTs) used for the design as reported by the Quartus II software.

Altera Structured ASIC Implementation Summary

Target Device Family	Complexity	Performance
Hardcopy II	24,000 to 37,500 HCells	314Mhz

Deliverables

- Graphical Configuration Java Tool
- Verilog Synthesizable RTL HDL
- Behavioral Verilog Models, Verilog testbenches with comprehensive Verification and regression test suite
- Synthesis Scripts for Altera Quartus II
- Direct technical support from MorethanIP Development team

Development Boards

- Standard Stratix II, Stratix III, Arria GX, Cyclone III, Stratix II and Stratix IIGX FPGA Prototyping / Development Boards
- Comprehensive 10/100 and 10/100/1000 Ethernet PHY board Selection

Ordering Code

MTIP-10_100_1000_MAC-lang-arch

Technology code

Language code

Language Code	*Delivery Language*
VHDL	Synthesizable RTL VHDL Source Code.
VLOG	Synthesizable RTL Verilog Source Code.
BIN	Encrypted RTL for Altera FPGA technology.

Technology Code	*Target Technology*
GEN	Generic sythesizable code for ASIC or FPGA implementations
ALTR	Synthesizable code optimized Altera FPGAs.

Contact

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