Tri-Mode (10/100/1000Mbps Ethernet) MAC Core

Features Summary

- Full Featured Tri-Mode, 10/100 and Gigabit MAC with integrated FIFO
- All Modes at all speeds UNH certified
- Silicon Proven on eASIC Nextreme™ 90nm Structured ASIC

Implementation Summary	
Families Supported	Nextreme™
Design File Formats	Verilog, VHDL, RTL, HDL
Verification	Testbench, Test-vectors
Support	MoreThanIP

Introduction

Ethernet is available in different speeds (10/100/1000 and 10000Mbps) It provides ubiqutous connectivity to meet a wide range of needs from desktop PCs to switches. MorethanIP provides solutions for each Ethernet application with a library of configurable MAC (Media Access Control) and PCS (Physical Coding Sub-layer) Cores.

The Tri-Mode Ethernet MAC core supports multiple applications including line cards, NIC cards and switching.
It supports Full-Duplex Mode including transparent (for switching applications) and full Ethernet frame termination/generation (for NIC or line card applications).

For efficient power management, the Core also implements Magic Packets detection.

The Tri-Mode Ethernet core seamlessly connects to any industry standard Gigabit Ethernet PHY device via a Gigabit Medium Independent Interface (GMII for 1000Mbps application) or Medium Independent Interface (MII for 10/100Mbps applications). The core connects to a user application via a SOC (System on a Chip) interface, which provides seamless connectivity to any MorethanIP cores such, or third party Core.

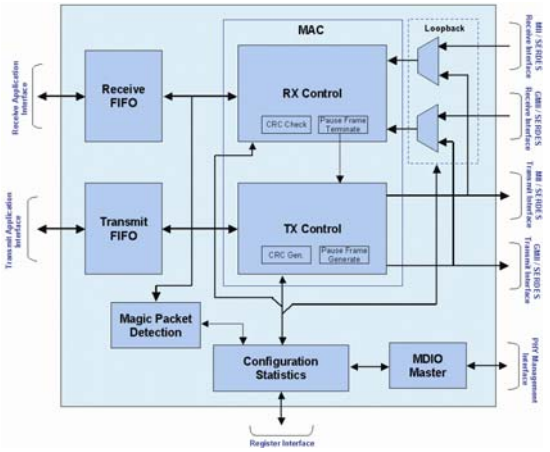


Figure 1. 10/100/1000 Ethernet MAC Core Block Diagram

MorethanIP also provides 1000Base-X PCS (Physical Coding Sublayer) Core and SGMII, RMII, RGMII, SSSMII modules to implements low pin count interfaces.

The Tri-Mode Ethernet MAC Core is fully UNH certified and is interoperable with major PHY vendor and systems.

10/100/1000 Ethernet MAC Core Features Overview

- Implements the full 802.3 specification with preamble / SFD generation, frame padding generation, CRC generation and checking on transmit and receive respectively
- Dynamically configurable to support 10Mbps, 100Mbps or 1Gbps operation
- Supports AMD Magic Packet detection for node remote power management
- Supports, for 10/100Mbps operation, full duplex or half duplex operation selectable via a Core configuration option
- Simple 8 or 32-Bit FIFO interface to Client application
- Implements fully automated XON and XOFF Pause Frame (802.3 Annex 31A) generation and termination
- Pause frame generation controllable by user application offering flexible traffic flow control
- In half-duplex mode, provides full collision support, including jamming, backoff, and automatic retransmission
- Support for VLAN tagged frames according to IEEE 802.1Q
- Programmable MAC address: Insertion on transmit; discards frames with mismatching destination address on receive (Except Broadcast and frames)
- Programmable group of four supplemental MAC addresses that can be used to accept / reject Unicast traffic
- Programmable Promiscuous mode support to omit MAC destination address checking on receive
- Multicast address filtering on receive based on 64 entries hash table reducing higher layer processing load
- Programmable frame maximum length providing support for any standard or proprietary frame length (e.g. 9K-Bytes Jumbo Frames)
- Optional internal GMII / MII Loopback
- Optional automatic receive errored frame discard
- Separate status word available for each received frame on the user interface providing information such as frame length, frame type, VLAN tag and error information
- MDIO Master interface for PHY device configuration and management with two programmable MDIO base addresses
- Optional statistics 32-Bit counters for IEEE 802.3 basic and mandatory Management Information Database (MIB) package as well as Ethernet MIB (RFC 2665) and Remote Network Monitoring (RFC 2819)

Deliverables

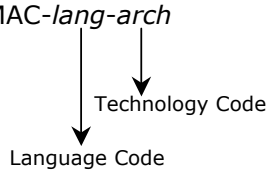
- Verilog or VHDL RTL HDL
- Behavioral Verilog models and Verification test cases
- Support for eASIC design tools
- Synthesis Scripts for Synopsys Design Compiler

Development and Evaluation Platforms

- Comprehensive 10/100 and 10/100/1000 Ethernet PHY Selection
- eASIC Nextreme kit part

Ordering Code

MTIP-10_100_1000_MAC-*lang-arch*



Language Code	Target Technology
VHDL	Synthesizable VHDL source code
VLOG	Synthesizable Verilog source code

Technology Code	Target Technology
NXTM	eASIC® Nextreme™ 90nm

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