10/100/1000Mbps Ethernet MAC Core

Version 3.65 - September 2007

Introduction

Ethernet is available in different speeds (10/100/1000 and 10000Mbps) and provides connectivity to meet a wide range of needs from desktop to switches. MorethanIP IP solutions provide a solution for each Ethernet application with a library of configurable MAC (Media Access Control) and PCS (Physical Coding Sub-layer) Cores.

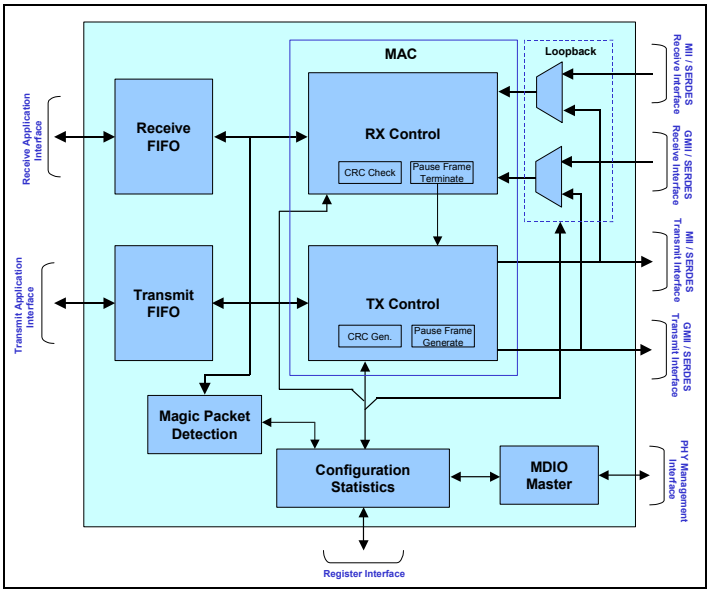
The programmable 10/100/100 Ethernet MAC from MorethanIP provides, with a single IP Core, a solution for Ethernet applications (Line Card, NIC card or switching) operating at 10/100 or 1000Mbps (Gigabit Ethernet). The 10/100/1000 MAC Core operates Full Duplex mode, supports transparent (For switching applications) and full Ethernet frame termination / generation (For NIC or line cards applications).

For efficient power management, the Core also implements Magic Packets detection.

The core can seamlessly connect to any industry standard Gigabit Ethernet PHY device via a Gigabit Medium Independent Interface (GMII for 1000Mbps application) or Medium Independent Interface (MII for 10/100Mbps applications) and to a user application via a SOC (System on a Chip) interface, which provides seamless connectivity to any MorethanIP cores such, or third party Core.

MorethanIP can also provide 1000Base-X PCS (Physical Coding Sublayer) Core and SGMII, RMII, RGMII, SSSMII modules to implements low pin count interfaces.

The Core is fully UNH certified and is interoperable with major PHY vendor and systems.



10/100/1000Mbps Ethernet MAC Core Overview

10/100/1000Mbps Ethernet MAC core Features

- Implements the full 802.3 specification with preamble / SFD generation, frame padding generation, CRC generation and checking on transmit and receive respectively
- Dynamically configurable to support 10Mbps, 100Mbps or 1Gbps operation
- Supports AMD Magic Packet detection for node remote power management
- Supports, for 10/100Mbps operation, full duplex or half duplex operation selectable via a Core configuration option
- Simple 8 or 32-Bit FIFO interface to Client application
- Implements fully automated XON and XOFF Pause Frame (802.3 Annex 31A) generation and termination
- Pause frame generation controllable by user application offering flexible traffic flow control
- In half-duplex mode, provides full collision support, including jamming, backoff, and automatic retransmission
- Support for VLAN tagged frames according to IEEE 802.1Q
- Programmable MAC address: Insertion on transmit; discards frames with mismatching destination address on receive (Except Broadcast and frames)
- Programmable group of four supplemental MAC addresses that can be used to accept / reject Unicast traffic
- Programmable Promiscuous mode support to omit MAC destination address checking on receive
- Multicast address filtering on receive based on 64 entries hash table reducing higher layer processing load
- Programmable frame maximum length providing support for any standard or proprietary frame length (e.g. 9K-Bytes Jumbo Frames)
- Optional internal GMII / MII Loopback
- Optional automatic receive errored frame discard
- Separate status word available for each received frame on the user interface providing information such as frame length, frame type, VLAN tag and error information
- MDIO Master interface for PHY device configuration and management with two programmable MDIO base addresses
- Optional statistics 32-Bit counters for IEEE 802.3 basic and mandatory Management Information Database (MIB) package as well as Ethernet MIB (RFC 2665) and Remote Network Monitoring (RFC 2819)

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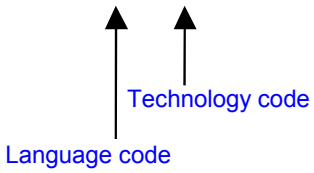
Implementation Summary

Xilinx FPGA Implementation Summary

Core Specifics		
Supported Device Family	Spartan 3E / Virtex 5 / Virtex 4	
Version	3.6	
Resources Used		
	Min	**Max**
LUTs	1472	2850
FFs	1981	3000
Block RAM	3	User Setting Dependent
Provided with Core		
Documentation	Datasheet, User Guide	
Design File Formats	Source RTL VHDL or Verilog Encrypted RTL VHDL or Verilog	
Constraints File	UCF File	
Verification	VHDL or Verilog Self-Checking Testbench	
Supported Design Tools		
Xilinx Tool	9.2i or Later	
Simulation	Modelsim 5.7 or Later	
Synthesis	XST	
Required Speed Grade		
Virtex 5	-1	
Virtex 4	-10	
Spartan-3E	-5	

Ordering Code

MTIP-10_100_1000_MAC-lang-arch



Language Code

Language Code	Delivery Language
BIN	Encrypted VHDL / Verilog Sources Code for Xilinx FPGAs.
VHDL	Synthesizable generic VHDL source code for Xilinx FPGA or ASICs implementations
VLOG	Synthesizable generic Verilog source code for Xiinx FPGAs or ASIC implementations

Technology Code

Technology Code	Technology
GEN	Source code option for FPGA, Structured ASICs and ASICs.
XLNX	Encrypted RTL for Xilinx FPGAs.

Contact

MorethanIP

E-Mail : info@morethanip.com
Internet : www.morethanip.com
Muenchner Strasse 199
D-85757 Karlsfeld
Germany

Tel : +49 (0) 8131 333939 0
FAX : +49 (0) 8131 333939 1

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