Product Brief
Version 1.1 - December 2002

1 Introduction

With the deployment of Fast Ethernet to the desktop, Gigabit Ethernet has become the standard backbone link to connect workgroup switches to backbone switches or access routers.

The IEEE802.3 specification defines, in Clause 36, a family of Physical Coding Sublayers (PCS) collectively known as 1000Base-X. It covers three embodiments within this family:

- 1000Base-CX for two pairs balanced copper cabling,
- 1000Base-LX for long wavelength optical transmission
- 1000Base-SX for short wavelength optical transmission.

The 1000Base-X PCS Core is compliant with Clause 36 of the IEEE802.3 standard and implements 8B/10B coding, link synchronization, frame encapsulation generation / termination. The Core also supports Auto-Negotiation (Clause 37 of IEEE802.3 standard), which is used to automatically, or under user application software control, exchange ability information between the Core and the remote end of the link and configure the Core to take the best advantage on the advertised features of the Remote node.

The core can seamlessly connect to any industry standard Gigabit Ethernet SERDES (SERializer / DESerializer) device via a Gigabit TBI (Ten Bit Interface) and to MAC Layer device with a standard GMII (Gigabit Medium Independent Interface) or an industry standard RGMII (Reduced Gigabit Medium Independent Interface), which provides a low pin, count 5-Bit DDR (Dual Data Rate) interface that is typically implemented in Ethernet Layer 2 switches devices.

The Core implements a PHY Management interface with control and management registers as define in Clause 22 of the IEEE 802.3 specification. The Core management interface address can be set via an external 5-Bit address bus and a LED control interface can be used to monitor kink synchronization and carrier sense.

Optionally a PMA (Physical Medium Attachment) SERDES is integrated in the Core when the solution is implemented in Altera Stratix GX devices. Using Stratix GX embedded SERDES features provides a highly integrated solution, which reduces board complexity and system cost.

The core is optionally delivered in generic synthesizable HDL (VHDL or Verilog) code (For use in Altera CPLD or ASIC technologies), or as a CPLD netlist, which provides a lower cost IP solution.

2 1000Base-X PCS core Features

- Implements Clause 36 of 802.3-2000 specification for 1000Base-X family of PCS (Physical Coding Sub-layer)
- Implements PCS frame encapsulation / de-encapsulation with /S/, /T/ orderset insertion / termination and /I/ Idle ordered set generation during inter-packet gap
- Implements receive link synchronization state machine and 10-Bit data alignment from SERDES with K28.5 character detection
- Link coding implemented with 8B/10B providing DC balanced bitstream for efficient SERDES operation
- Implement User controllable 1000Base-X Auto-Negotiation (IEEE 802.3 Clause 37) which fully programmable node ability register
- Link timer used during Auto Negotiation programmable via the Core PHY Management interface using a MorethanIP specific management register
- Optional PMA (Physical Medium Attachment) SERDES when implemented in Altera Stratix GX devices
- Optional serial 1.25Gbps MDI (Medium Dependent Interface) implemented with Altera Stratix GX embedded SERDES
- MDIO Slave PHY Management interface which provides a standard interface for Core configuration and management
- Implements standard management register set as defined in Clause 22 of IEEE802.3 which specific Extended registers for improved flexibility
- Supports PHY isolation support to allow the implementation of a Hot Swappable PHY device and provides control to for technology specific powerdown
- PHY serial loopback support with standard MDIO command register
- Programmable physical MDIO address via an external 5-Bit address
- Programmable (Via PHY Management interface) GMII Loopback mode available for system test
- Can be implemented in Altera CPLDs or ASICs
- Can optionally be delivered in VHDL or Verilog source code or netlist which provides a lower cost licensing option
- Design Kit contains extensive Ethernet frame generators and checking models enabling fully automated design verification and testing for standard compliance and error behavior, enabling for fast turn-around design cycles

3 Block Diagram

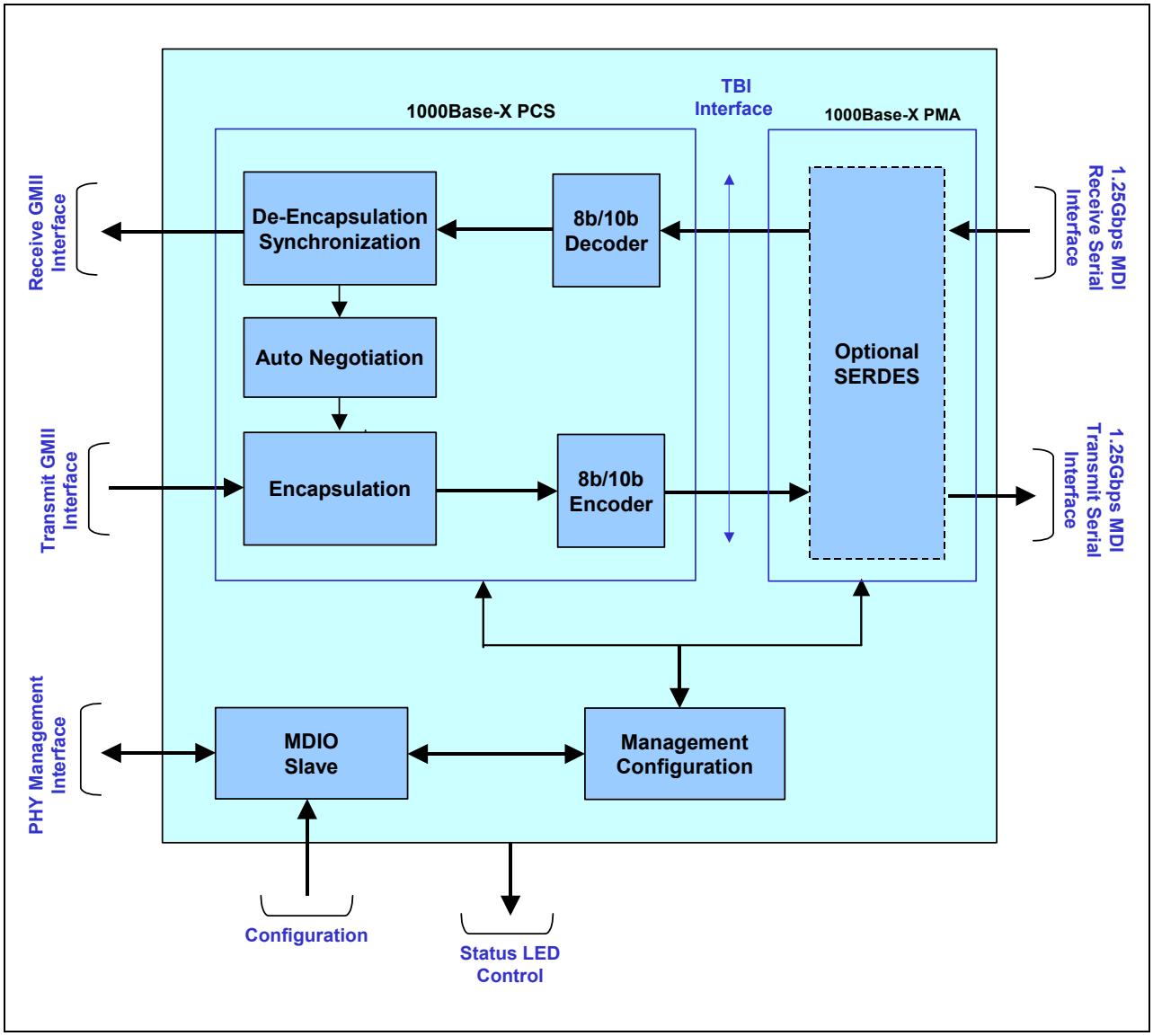

Figure 1: 1000Base-X PCS Core Block Diagram

4 Implementation Summary

Table 1: 1000Base-X PCS Core Complexity Summary

Target Device Family	Speed Grade	Complexity (With 256 Bytes FIFOs) LEs	Performance	Requirement
STRATIX (EP1S10)	-7	1040	140MHz	125MHz
STRATIX GX (EP1SGX10)	-7	820	145MHz	125MHz
CYCLONE (EP1C12)	-8	1050	128MHz	125MHz

5 1000Base-X PCS Core Design Kit Overview

Table 2: Design Kit Overview

Design and Simulation	
Language	Optimized VHDL / Verilog or lower cost CPLD encrypted netlist.
Simulation	Configurable VHDL / Verilog Testbench with embedded frame generator and checker providing an easy to use and robust de-bugging environment.
Verification	Comprehensive test environment with Ethernet frame generator and verification models for standard compliant and errored frame generation and automated core behavior verification.
Supported Design Tools	
Simulation	Modelsim Version 5.6 or higher.
Synthesis	Synplify v6.3.1. or higher Leonardo Spectrum v2002.1e or higher Synopsys Design Compiler
Implementation	Altera Quartus II Version 2.2 or higher

6 References

1. IEEE 802.3 2002 Edition

7 Ordering Code

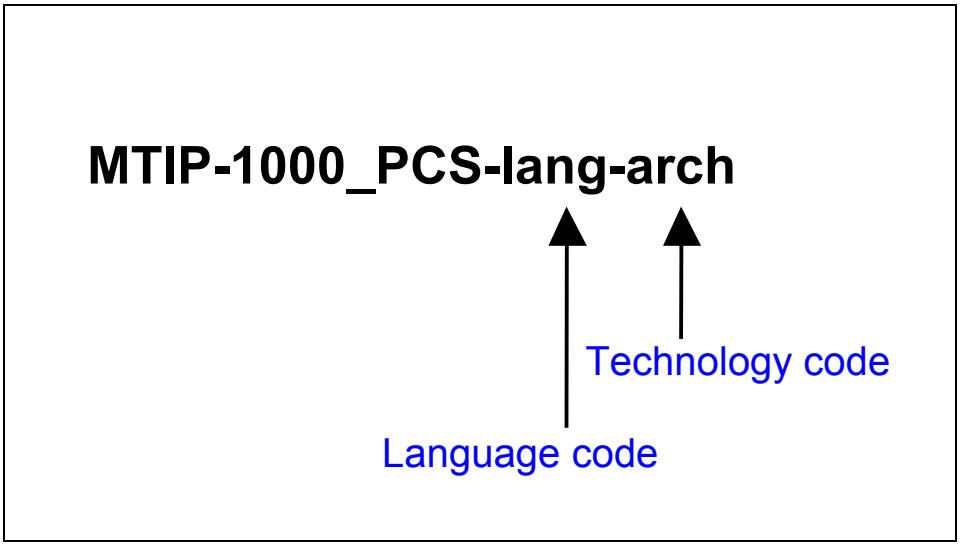

Table 3: Language Code

Technology Code	Target Technology
BIN	Encrypted CPLD netlist.
VHDL	Synthesizable generic VHDL source code for CPLD or ASIC implementations
VLOG	Synthesizable generic Verilog source code for CPLD or ASIC implementations

Table 4: Technology Code

Technology Code	Target Technology
GEN	Source code option for Altera CPLDs (CYCLONE, STRATIX or STRATIX GX) or ASIC implementations.
ALTR	Encrypted netlist for Altera CPLDs (CYCLONE, STRATIX or STRATIX GX).

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