QSGMII PCS Core Product Brief

Version 1.0 - July 2009

Introduction

With the deployment of Fast Ethernet to the desktop, Gigabit Ethernet has become the standard backbone link to connect workgroup switches to backbone switches or access routers.

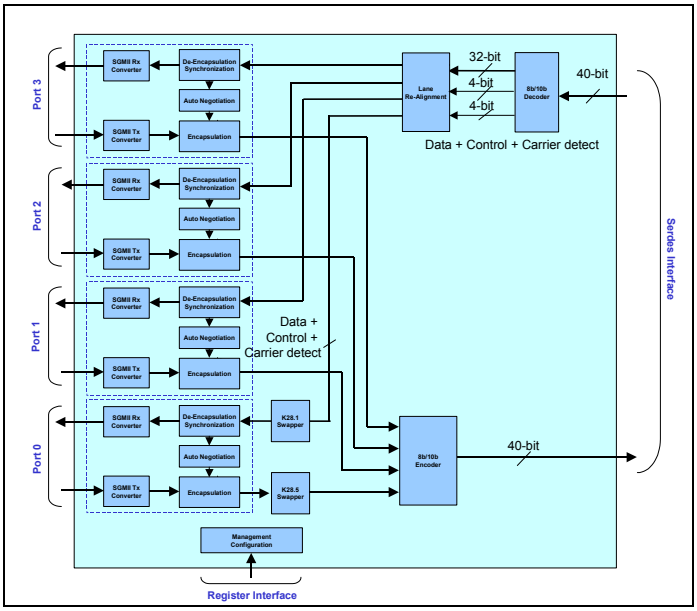
The SGMII (Serial GMII) specification is an industry standard that uses the underlying standard PCS function to also support 10/100 Ethernet, with data duplication, with a serial 1.25Gbps serial link.

To reduce the number of I/Os when multiple ports are implemented, the QSGMII (Quad Serial GMII) interface combines four SGMII interfaces into a single serial interface running at 5Gbps.

MorethanIP QSGMII PCS Core implements 8B/10B coding, link synchronization, frame encapsulation generation / termination compliant with Clause 36 of the IEEE802.3 standard and adapted to the Cisco QSMII specification version 1.2.

The Core also supports SGMII Auto-Negotiation, extended from Clause 37 of the IEEE802.3, which is used to automatically, or under user application software control, exchange ability information between the Core and the remote end of the link and configure the Core to take the best advantage on the advertised features of the Remote node.

The core is optionally delivered in generic synthesizable HDL (VHDL or Verilog) code (For use in Altera FPGA or ASIC technologies), or as a FPGA netlist, which provides a lower cost IP solution.



QSGMII PCS Core Block Diagram

QGMII PCS Core Features Overview

- Compliant with Cisco QSGMII specification version 1.2 and implements four 10/100/1000 links
- Implements Clause 36 of 802.3-2002 specification for 1000Base-X family of PCS (Physical Coding Sub-layer) for encapsulation, line encoding and link synchronization
- Implements PCS frame encapsulation / de-encapsulation with /S/, /T/ ordered set insertion / termination and /I/ Idle ordered set generation during inter-packet gap
- Modified transmitter on for port 0 to only transmit /I1/ Idle ordered set
- Implements receive link synchronization state machine and 10-Bit data alignment from SERDES with K28.1 and K28.5 character detection
- Implements SGMII converter to support 10/100 or Gigabit operation for each port
- Implements QSGMII K28.5 swapper on port 0 transmit and K28.1 swapper on Port 0 receive to support four MII / GMII ports.
- Link coding implemented with 8B/10B providing DC balanced bitstream for efficient SERDES operation
- Programmable Decoder running disparity checking disable
- Implements QSGMII Auto-Negotiation (Cisco Specification) for Port 0 and SGMII Auto-Negotiation (Cisco Specification) for all other ports.
- Auto-Negotiation Link timer programmable via the Core PHY Management interface using a MorethanIP specific management register
- Implements standard management register set as defined in Clause 22 of IEEE802.3 which specific Extended registers providing improved flexibility
- Supports PHY isolation support to allow the implementation of a Hot Swappable PHY device
- Programmable (Via PHY Management interface) QSGMII serial Loopback mode available for system test for each port.
- Integrated with Altera Arria II GX and Stratix IV GX/GT embedded Serdes
- Can optionally be delivered in VHDL or Verilog source code or netlist which provides a lower cost licensing option

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Implementation Summary

Altera FPGA Implementation Summary

Target Device Family	Speed Grade	Complexity		
		ALUTs	Registers	Memory
Stratix IV GT	C4/I4	2930	3615	1328 Bits
Stratix IV GX				
Arria II GX	C6/I6	2890	3395	1328 Bits

Deliverables

- Verilog / VHDL Synthesizable RTL HDL or encrypted RTL for FPGA implementation
- Behavioral Verilog or VHDL testbenches and Verification test cases
- SDC timing constraint file
- Support for FPGA and ASIC design tools
- Supported directly by MorethanIP engineers

Ordering Code

MTIP-QSMII_PCS-lang-tech

technology code

language code

Language Code	*Delivery Language*
VHDL	Synthesizable RTL VHDL Source Code.
VLOG	Synthesizable RTL Verilog Source Code.
BIN	Encrypted RTL for Altera FPGA technology.

Technology Code	*Target Technology*
GEN	Generic sythesizable code for ASIC or FPGA implementations
ALTR	Synthesizable code optimized Altera FPGAs.

Contact

MorethanIP

E-Mail : info@morethanip.com

Internet : www.morethanip.com

Muenchner Strasse 199

D-85757 Karlsfeld

Germany

Tel : +49 (0) 8131 333939 0

FAX : +49 (0) 8131 333939 1