Product Brief
V1.2 - May 2009

1 Introduction

With the deployment of Fast Ethernet to the desktop, Gigabit Ethernet has become the standard backbone link to connect workgroup switches to backbone switches or access routers.

The IEEE802.3 specification defines, in Clause 36, a family of Physical Coding Sublayers (PCS) collectively known as 1000Base-X. It covers three embodiments within this family:

- 1000Base-CX for two pairs balanced copper cabling,
- 1000Base-LX for long wavelength optical transmission
- 1000Base-SX for short wavelength optical transmission.

The 1000Base-X PCS Core is compliant with Clause 36 of the IEEE802.3 standard and implements 8B/10B coding, link synchronization, frame encapsulation generation / termination. The Core also supports Auto-Negotiation (Clause 37 of IEEE802.3 standard), which is used to automatically, or under user application software control, exchange ability information between the Core and the remote end of the link and configure the Core to take the best advantage on the advertised features of the Remote node.

The PCS Core can be used with SGMII PHYs, supports SGMII 10/100 or Gigabit operation with data duplication and SGMII Auto-Negotiation according to the Cisco specification.

The core can seamlessly connect to any industry standard Gigabit Ethernet SERDES (SERializer / DESerializer) device via a Gigabit TBI (Ten Bit Interface) and to MAC Layer device with a standard GMII (Gigabit Medium Independent Interface) for Gigabit operation or MII (Medium Independent Interface) for 10/100Mbps operation.

The core is optionally delivered in generic synthesizable HDL (VHDL or Verilog) code (For use in Altera FPGA or ASIC technologies), or as a FPGA netlist, which provides a lower cost IP solution.

2 SGMII PCS Core Features

- Implements Clause 36 of 802.3-2000 specification for 1000Base-X family of PCS (Physical Coding Sub-layer)
- Implements PCS frame encapsulation / de-encapsulation with /S/, /T/ ordered set insertion / termination and /I/ Idle ordered set generation during inter-packet gap
- Implements receive link synchronization state machine and 10-Bit data alignment from SERDES with K28.5 character detection
- Implements SGMII converter to support 10/100 or Gigabit operation
- Link coding implemented with 8B/10B providing DC balanced bitstream for efficient SERDES operation
- Implement User controllable 1000Base-X Auto-Negotiation (IEEE 802.3 Clause 37) with fully programmable node ability register
- Optionally implements SGMII Auto-Negotiation (Cisco Specification)
- Link timer, used during standard or SGMII Auto-Negotiation, programmable via the Core PHY Management interface using a MorethanIP specific management register
- Implements standard management register set as defined in Clause 22 of IEEE802.3 which specific Extended registers providing improved flexibility
- Supports PHY isolation support to allow the implementation of a Hot Swappable PHY device
- Programmable (Via PHY Management interface) GMII Loopback mode available for system test
- Encapsulation and auto negotiation functions can optionally be by-passed
- Can be implemented in Altera FPGAs or ASICs
- Can optionally be delivered in VHDL or Verilog source code or netlist which provides a lower cost licensing option
- Design Kit contains extensive Ethernet frame generators and checking models enabling fully automated design verification and testing for standard compliance and error behavior, enabling for fast turn-around design cycles

3 Core Block Diagram

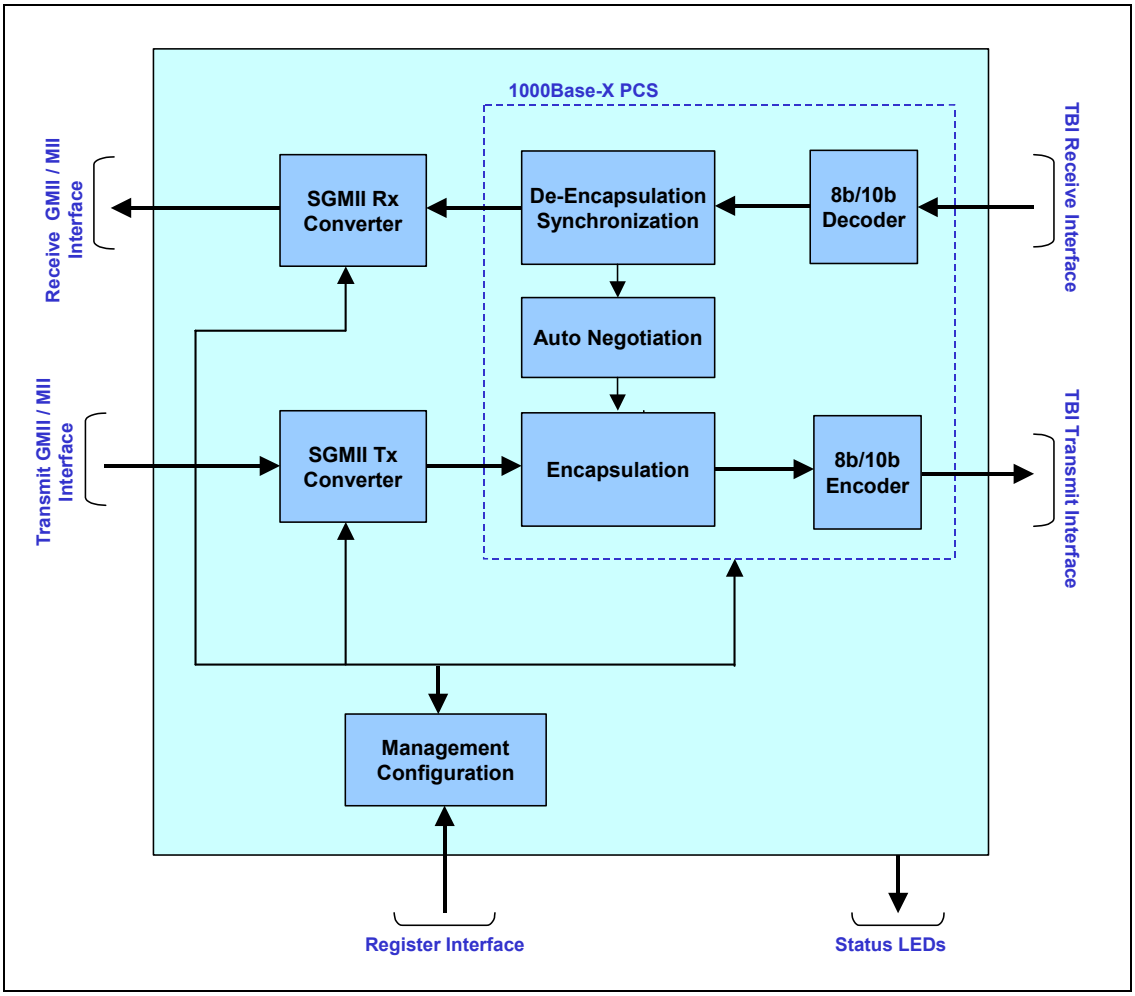

Figure 1: 10/100/1000 SGMII PCS Core Overview

4 Implementation Summary

Table 1: SGMII PCS Core complexity Summary

Target Device Family	Speed Grade	Complexity	Performance	Requirement
STRATIX II	-5	880 LEs (1)	170MHz	125MHz
STRATIX III	-4	1000 LEs (1)	190MHz	12MHz
CYCLONE II	-8	1250 LEs	140MHz	125MHz
CYCLONE III	-8	1500 LEs	130MHz	125MHz
STRATIX II GX	-5	880 LEs (1)	150MHz	125MHz
STRATIX IV	-4	800 LEs (1)	220MHz	125MHz
ARRIA II GX	-6	880 LEs (1)	150MHz	125MHz

1. The Logic Element count for Stratix II and Stratix III devices is based on the number of adaptive look-up tables (ALUTs) used for the design as reported by the Quartus II software.

5 Core Design Kit Overview

Table 2: Design Kit Overview

Design and Simulation	
Language	VHDL / Verilog Source Code or Encrypted VHDL / Verilog Sources Code for Altera FPGAs.
Simulation	Configurable VHDL / Verilog Testbench with embedded frame generator and checker providing an easy to use and robust de-bugging environment.
Verification	Comprehensive test environment with Ethernet frame generator and verification models for standard compliant and errored frame generation and automated core behavior verification.
Supported Design Tools	
Simulation	Modelsim Version 5.7a or higher.
Synthesis	Altera Quartus II V9.0 or Higher
Implementation	Altera Quartus II V9.0 or Higher

6 References

1. IEEE 802.3 2002 Edition

7 Ordering Code

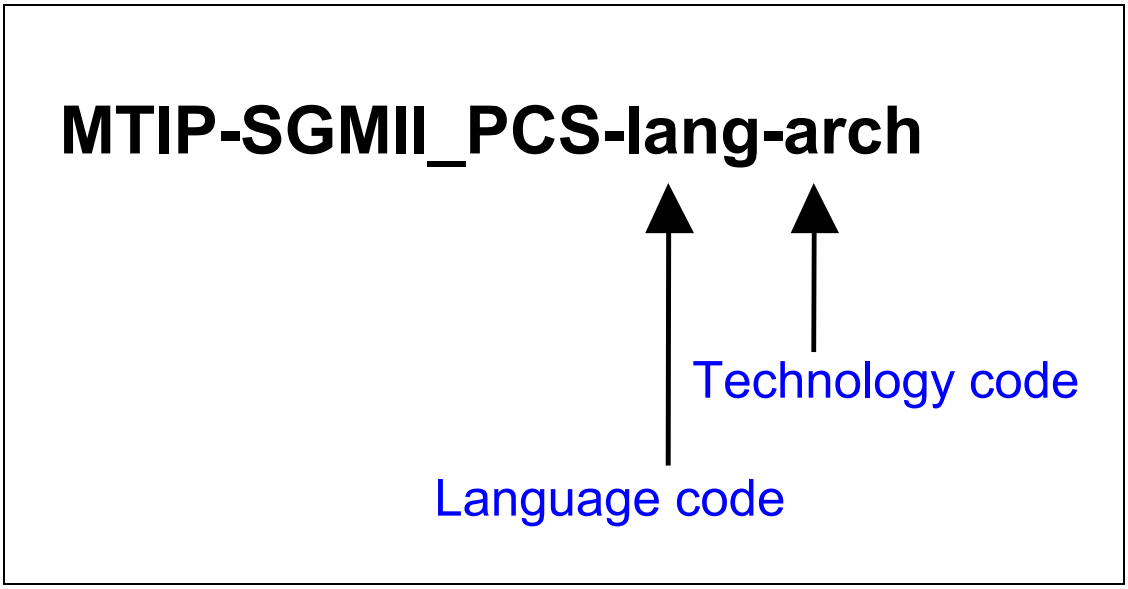

Table 3: Language Code

Technology Code	Target Technology
BIN	Encrypted FPGA netlist.
VHDL	Synthesizable generic VHDL source code for FPGA or ASIC implementations
VLOG	Synthesizable generic Verilog source code for FPGA or ASIC implementations

Table 4: Technology Code

Technology Code	Target Technology
GEN	Source code option for Altera FPGAs or ASIC implementations.
ALTR	Encrypted netlist for Altera FPGAs.

8 Contact

MorethanIP

E-Mail : info@morethanip.com

Internet : www.morethanip.com

Muenchner Str. 199

D-85757 Karlsfeld

Germany

Tel : +49 (0) 8131 333939 0

FAX : +49 (0) 8131 333939