3-Port Ethernet Switch with 1588 and Cut-Through Product Brief

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Introduction

An Ethernet switch is used to interconnect a number of Ethernet stations, forming an Ethernet network. Different ports of the switch can be connected to different network segments or individual nodes. The switch learns the MAC addresses observed from frames received through each port and uses this information to forward incoming frames only to the intended destination instead of flooding the network.

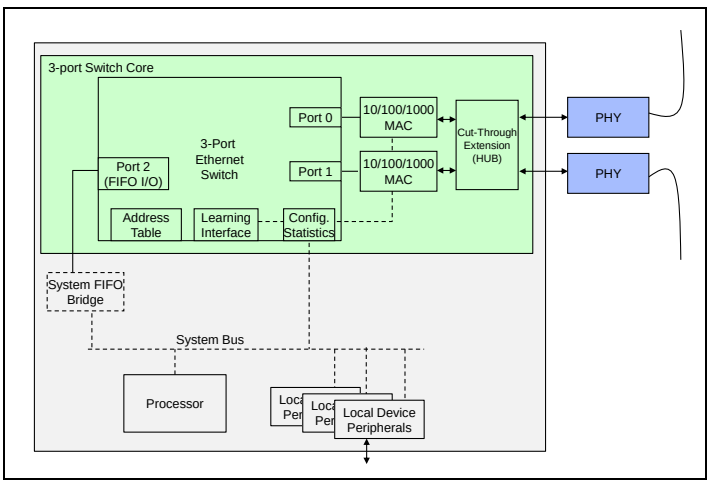
The 3-Port Ethernet switch core is typically integrated into a device allowing for daisy-chain or ring network topologies. Each node implements a local port that enables it to transfer frames to and from the network. The switching function takes care on passing frames on or bypassing the node for traffic not relevant to the local device.

The 3-Port Ethernet Switch core implements two 10/100 or 10/100/1000 Ethernet MACs allowing direct connection to external PHY devices through standard interfaces like MII or GMII. The 3rd port offers a flexible FIFO interface for integration into any system environment.

For precise time synchronization applications, the switch and MAC functions support frame timestamping and IEEE 1588v2 correction field updates. A dedicated adjustable timer module is integrated that can be used to provide precise timestamps and system time to the application.

Optionally a configurable Cut-Through function is available on the line ports allowing very low latency forwarding of traffic that is not intended for the local device.

The Core is delivered either in generic Verilog synthesizable HDL code for ASIC and FPGA implementations, or in an encrypted format for FPGA implementations.



3-Port Switch Device Integration Example

3-Port Switch Main Features

- Ethernet switch engine with 3 ports supporting gigabit bandwidth
- Integrated Ethernet MACs on two ports with MII or GMII or their reduced variants (RMII, RGMII) as needed
- Local port with generic 32bit FIFO interface for flexible system interconnect or alternatively application specific system bridge
- Full-duplex line rate support at all speeds and optionally half-duplex operation for 10/100 networks
- MAC address table with 256 entries and option to extend it to up to 2048 entries.
- Software controlled learning and aging for flexible address table management
- Support for VLAN tagged frames according to IEEE 802.1Q specification with configurable VLAN verification and support for up to 32 VLAN domains
- Priority classification and configurable remapping using VLAN priority or IP layer Diffserv/COS fields
- QoS Support implementing 4 output queues per port
- Strict priority or weighted fair queuing selection for queues
- Programmable frame maximum length up to 1700 byte
- Configurable Multicast and Broadcast masks for flooding control
- Management Frame (BPDU) filtering and special forwarding capabilities to support network management protocol implementations
- Optional reduced or full statistics counters for IEEE 802.3 basic and mandatory Management Information Database (MIB) package as well as Ethernet MIB (RFC 2665) and Remote Network Monitoring (RFC 2819)
- TX/RX timestamping enabling IEEE 1588 applications
- Automatic 1-step correction field update for IEEE 1588v2 Layer 2 frames for transparent clock support
- Integrated software adjustable timer module providing seconds and nanoseconds values
- Two integrated Clause 22 MDIO master controllers for PHY management on the external ports
- Optional Cut-Through function on external ports for size independent and reduced latency (<3µs at 100Mbps) on traffic that needs to traverse the node
- Optional Mirroring and Snooping functions for use by network and application management protocols
- Optional support for Device Level Ring (DLR) processing beacon frames in hardware

Implementation Summary

Target Device Family	Complexity (option dependent)	Memory (bits) (256 addresses)	Performance
ASIC	~150K - 200K gates ~20000 DFFs	250Kbit	> 200 MHz
FPGA e.g. Altera Cyclone-III/IV/V	~19000 - 23000 LEs	320Kbit	>140MHz

Deliverables

- Verilog Synthesizable RTL or encrypted RTL for FPGA implementation
- Behavioral Verilog testbenches and Verification test cases
- Support for FPGA and ASIC design tools

Ordering Code

MTIP-P3SX1588-opt-lang-tech

Opt Code	*Description*
std	Normal Store&Forward switch
hub	With Cut-Through HUB extension

Language Code	*Delivery Language*
VLOG	Synthesizable RTL Verilog Source Code.
BIN	Encrypted RTL for FPGA technology.

Technology Code	*Target Technology*
GEN	Generic sythesizable code for ASIC or FPGA implementations
ALTR	Synthesizable code for Altera FPGAs.
XIL	Synthesizable code for Xilinx FPGAs.

Contact

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