Ethernet Switch Core supporting 1588 and AVB
Product Brief

Version 2.0 - February 2012

Introduction

An Ethernet switch connects a number of Ethernet stations, forming an Ethernet network. Different ports of the switch can be connected to different network segments or individual nodes. The switch learns the MAC addresses observed from frames received through each port and uses this information to forward incoming frames only to the intended destination instead of flooding the network.

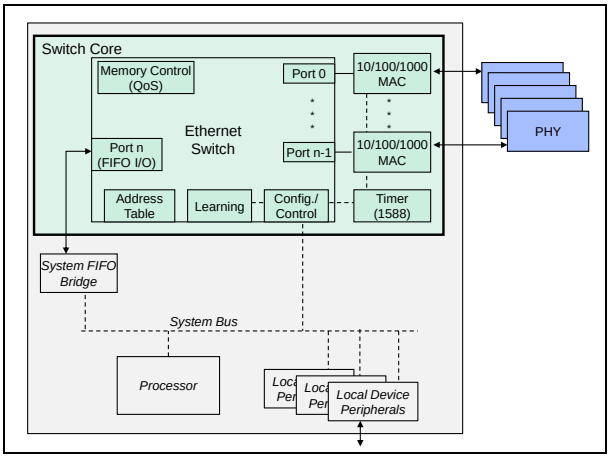
To support Audio Video Bridging (AVB) applications a switch classifies incoming frames to be treated with specific bandwidth requirements for forwarding. The classification defines two Stream Reservation (SR) classes, class A and class B whose bandwidth can be reserved for AV traffic. Bandwidth not allocated to AV traffic will be used by normal networking traffic respecting QoS and giving priority to AV.

The Ethernet switch core is typically integrated into a device (node) allowing for connection with a host processor which operates system management functions and implements higher layer data and protocol processing. The switching function takes care on passing frames on or bypassing the node for traffic not relevant to the local device.

The Ethernet Switch core integrates 10/100/1000 Ethernet MACs allowing direct connection to external PHY devices through standard interfaces like MII or GMII or their pin-reduced variants. One dedicated port offers a flexible FIFO interface for integration into any system environment.

For precise time synchronization applications, the switch and MAC functions support frame timestamping and IEEE 1588v2 correction field updates. A dedicated adjustable timer module is integrated that can be used to provide precise timestamps and system time to the application.

The Core is delivered either in generic Verilog synthesizable HDL code for ASIC and FPGA implementations, or in an encrypted format for FPGA implementations.



Switch Device Integration Example

Switch Core Main Features

- Flexible Ethernet switch engine with up to 11 ports with a shared total switching capacity of typically 2-6 Gbps (depending on target technology used).
- Integrated Ethernet MACs with MII or GMII or their reduced variants (RMII, SMII, RGMII, SGMII) as needed
- Local port with generic 32bit FIFO interface for flexible system interconnect or application specific system bridge
- Full-duplex line rate support at all speeds and optionally half-duplex operation for 10/100 networks
- MAC address table with up to 2048 entries.
- Fully hardware controlled learning and aging with flexible control for address table management allowing static and dynamic address entries
- Support for VLAN tagged frames according to IEEE 802.1Q specification with configurable VLAN verification and support for up to 32 VLAN domains
- Priority classification and configurable remapping using VLAN priority or IP layer Diffserv/COS fields
- QoS Support implementing 4 or 8 output queues per port
- Strict priority or weighted fair queuing selection for queues
- Configurable Parsers for AVB traffic classification and Credit Based Shaper (802.1Qav) bandwidth control
- Optional configurable Random Early Detection (RED) RFC 2309 congestion management on output queues
- Programmable frame maximum length up to 1700 byte
- Configurable Multicast and Broadcast flooding control
- Management Frame (BPDU) filtering and special forwarding capabilities to host processor port supporting network management protocol implementations
- Statistics counters for IEEE 802.3 basic Management Information Database (MIB) package, Ethernet MIB (RFC 2665) and Remote Network Monitoring (RFC 2819)
- Frame timestamping enabling IEEE 1588 (PTP) and 802.1as (AVB) applications
- Automatic 1-step correction field update for IEEE 1588v2 Layer 2 frames for transparent clock support
- Integrated software adjustable timer module providing seconds and nanoseconds values
- Integrated Clause 22 MDIO master controllers for PHY management on the external ports
- Optional Mirroring and Snooping functions for use by network and application management protocols

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Implementation Summary

Target Technology	Complexity for 4-Port Example 64Kbyte Buffer, 2048 address table	Complexity for 10-Port Example 64Kbyte Buffer, 2048 address table	Performance
ASIC	~300K - 400K gates ~900Kbit memory	~700K - 900K gates ~1.4Mbit memory	> 300 MHz
FPGA	~30000 LEs ~1Mbit memory	~55000 LEs ~1.4Mbit memory	>140MHz

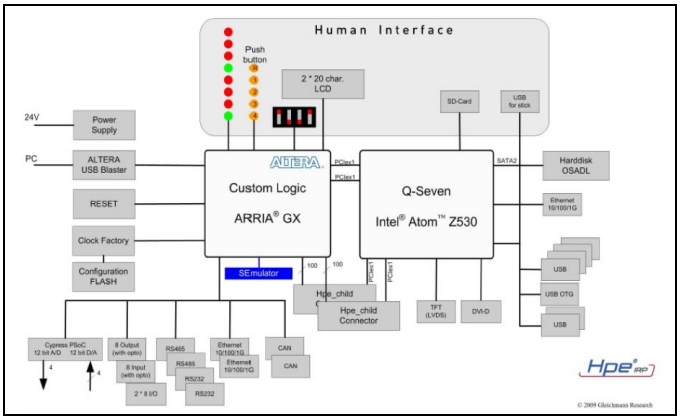
Deliverables

- Verilog Synthesizable RTL or encrypted RTL for FPGA implementation
- Behavioral Verilog testbenches and Verification test cases
- Support for FPGA and ASIC design tools

Prototyping

For application development and rapid prototyping a FPGA based reference platform is available. It allows implementing 3 to 5 Port switch configurations and uses an AMBA AHB slave bridge between the switch core and the system interconnect.

The platform integrates the switch core alternatively with an Atom or ARM based processor environment (Q-Seven module) and peripherals providing four Ethernet Ports with RJ45 sockets. The software environment implements the Linux operating system with networking drivers for the switch. Contact MorethanIP for more information.



Ordering Code

MTIP-P6SXAVB-lang-tech

Language Code	*Delivery Language*
VLOG	Synthesizable RTL Verilog Source Code.
BIN	Encrypted RTL for FPGA technology.

Technology Code	*Target Technology*
GEN	Generic synthesizable code for ASIC or FPGA implementations
ALTR	Synthesizable code for Altera FPGAs.
XIL	Synthesizable code for Xilinx FPGAs.

Contact

MorethanIP GmbH

E-Mail : info@morethanip.com
Internet : www.morethanip.com

Muenchner Strasse 199
D-85757 Karlsfeld
Germany
Tel : +49 (0) 8131 333939 0
FAX : +49 (0) 8131 333939 1

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