25/40/50 Gigabit Ethernet Base-R/KR PCS Core

Preliminary Product Brief Version 1.0 - July 2014

Introduction

The 25/40/50Gbps Ethernet PCS Core is compliant with the IEEE802.3ba 40G and Broadcom 25Gbps and 50Gbps Ethernet specifications allowing systems to support link speeds above 10Gbps, with no increase of the Trace and/or Cable interconnect density.

The 25Geth interface is implemented with a single 25Gbps Serdes Lane and the 50Geth interface with two 25Gbps Serdes Lanes.

The Core also supports standard 40Geth applications over four 10.3125Gbps Serdes lanes or two 20.6250Gbps Serdes lanes for trace and/or cable interconnect.

The Core implements standard 40Geth scrambler and descrambler, the 64b/66b encoder and decoder, multi-lane distribution (MLD), alignment marker insertion/striping and block synchronization.

The MLD module distributes data across 4 virtual lanes. The 4 virtual lanes are then transferred on 4x 10Gbps (40Geth) serial lanes, on 2x 20/25Gbps (40/50Geth) serial lanes or on 1x 25Gbps (25Geth) serial lane.

On receive, the MLD deskews the physical lanes producing an aligned 40Geth or 50Geth data stream. In 25Geth mode, the MLD just re-aligns the serial data stream.

The Core optionally supports the IEEE Clause 74 Firecode FEC and/or the IEEE Clause 91 Reed Solomon FEC (RS-FEC). The RS-FEC is used for 25 and 50Geth backplane applications over 25Gbps Serdes Lanes.

On the application side, the Core implements a 64-Bit XLGMII (40 Gigabit Media Independent Interface).

On the line side, the Core implements a flexible 16 to 32 or 64 bit parallel interface per lane. Each lane is connectable to Industry standard embedded 10.3125Gbps and 25.78125Gbps Serdes macros.

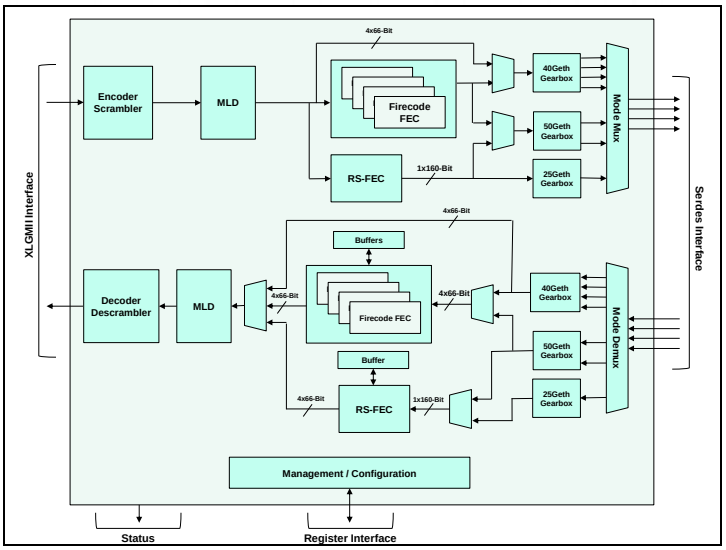
The PCS Core can be used with MorethanIP Link Training and Autonegotiation Cores to design flexible backplane interconnection solutions.

The MorethanIP Autonegotiation Core is fully generic and can support any proprietary 'Next Page' negotiations for selecting the 25Geth or 50Geth modes of operation.

The Core is delivered in generic synthesizable technology independent Verilog HDL code.

The Core is delivered with a comprehensive verification environment and expert MorethanIP technical and application support.

Block Diagram



Core Block Diagram

Core Features

- Compliant with IEEE802.3ba Clause 82 40G Ethernet and Broadcom 25Geth & 50Geth Specification Version 1.3
- Configurable Serdes PMA interface width
- Multi-Lane Distribution (MLD) across 4 Virtual Lanes with flexible multiplexing over 4 (40Geth), 2 (40/50Geth) or 1 (25Geth) Serdes lane
- Periodic Alignment Marker insertion / striping on transmit / receive, respectively
- 40Geth and 50Geth Lane deskew
- Implements 40 Gigabit Ethernet data Scrambler which generates transition rich signals to the application high speed optical link on the Core transmit path, and data De-Scrambler on the Core receive path
- 64b/66b Encoder / Decoder performing 66-bit block synchronization, 64b/66b receive path decoding, 64b/66b transmit path encoding, and 66b/64b transmit path conversion for block overhead bits
- Implements Bit Error Rate (BER) monitoring, with high error rate indication, providing constant line quality monitoring
- Optional Firecode FEC (Clause 74), RS-FEC (Clause 92) and Auto-Negotiation functions (Clause 73) for 25/40/50GBase-KR applications
- Optional support for Fast Wake and Deep Sleep Energy-Efficient Ethernet (EEE, 802.3bj) modes

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- Can be seamlessly connected to the MorethanIP Low Latency 64-Bit 25/40/50 Gigabit Ethernet MAC
- Optional Extended MDIO (Clause 45) serial Management Data Interface.
- Optional direct 16-bit host interface to access to the internal registers of the PCS (Instead of MDIO)

Implementation Summary - Preliminary

Modes		*Complexity*		
25Geth	***RS-FEC***	**x**		**x**
40Geth	***No FEC***	**x**	**x**	**x**
	Firecode FEC		**x**	**x**
50Geth	***Firecode FEC***		**x**	**x**
	RS-FEC	**x**		**x**
Gates		450K	190K	540K
Memory Bits		56,208	29,696	64,528

Deliverables

- Verilog Synthesizable RTL HDL
- Behavioral Verilog testbenches and Verification test cases
- Verilog Simulation regression suite
- Synthesis script for Synopsys Design Compiler
- Timing constraints is Synopsys SDC format
- Direct support by MorethanIP engineers

Ordering Code

MTIP-25_40_50G_PCS-lang-arch

Technology code

Language code

Language Code	*Delivery Language*
VLOG	Synthesizable RTL Verilog Source Code.

Technology Code	*Target Technology*
GEN	Generic synthesizable code for ASIC.

Contact

MorethanIP GmbH

E-Mail : info@morethanip.com

Internet : www.morethanip.com

Muenchner Strasse 199

D-85757 Karlsfeld

Germany

Tel : +49 (0) 8131 333939 0

FAX : +49 (0) 8131 333939 1