100GBase-KR4 / CR4 / SR4 / KP4 PCS Core

Product Brief
Version 1.1 - May 2015

Introduction

The 100 Gigabit Ethernet 100GBase-KR4 / CR4 / SR4 / KP4 PCS Core is compliant with the IEEE P802.3bj Specification and is designed to be used in conjunction with the MorethanIP 100 Gigabit MAC Core to create flexible system solutions for 100Gigabit Ethernet LAN applications.

The Core can also be used with embedded 50Gbps Serdes to implement a 100Geth interface over two Serdes lanes.

The Core implements the standard IEEE 802.3 Clause 82 scrambler / descrambler and the 64b/66b encoder / decoder.

The RS-FEC for 25Gbps and 50Gbps Serdes with NZR modulation uses RS(528, 514) codewords allowing correction of up to seven 10-Bit symbols within 514 symbols and the RS-FEC for 50Gbps Serdes with PAM4 modulation uses RS(544, 514) codewords allowing correction of up to 15 10-Bit symbols within 514 symbols.

With RS-FEC a MLD module distributes data across 4 virtual lanes. The 4 virtual lanes are then transcoded into RS-FEC codewords and transferred on the 25 / 50Gbps serial lanes.

On receive, the MLD re-aligns and deskew the serial data stream to the RS-FEC codeword boundaries for allowing error correction and decode.

The RS-FEC and FC-FEC error propagation to the PCS can be bypassed with software programming or can be removed with a synthesis option to reduce the Core latency.

On the application side, the Cores implement a 192-Bit CGMII (100 Gigabit Media Independent Interface) interface.

On the line side, the Core implements, per Serdes Lane, a flexible 80-bit parallel interface connectable to Industry standard embedded 25.78125Gbps, 51.5625Gbps NRZ or 53.1625Gbps PAM4 Serdes macros.

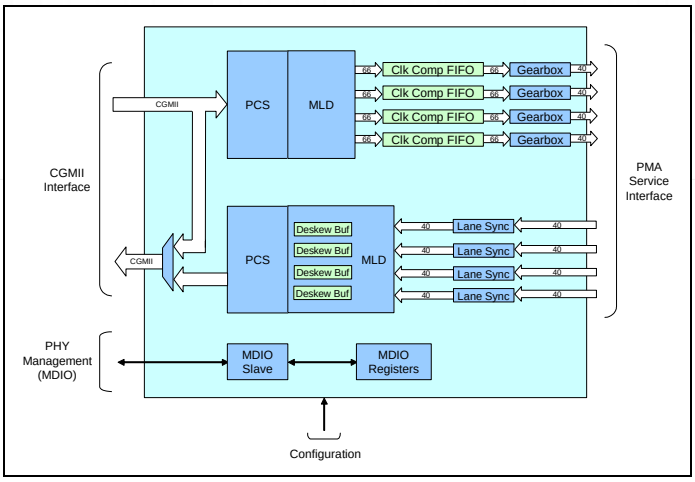
The PCS Core can be used with MorethanIP Link Training and Autonegotiation Cores to design flexible backplane interconnection solutions.

The Core is optimized for latency and can be used to design Synchronous Ethernet applications

The MorethanIP Clause 73 Autonegotiation Core is fully generic and supports 'Next Page' negotiations to select the, non IEEE, 100Geth over two Lane mode of operation.

The Core is delivered in generic synthesizable technology independent Verilog HDL code.

The Core is delivered with a comprehensive verification environment and expert MorethanIP technical and application support.



100GBase-KR4 / CR4 / SR4 / KP4 Core Block Diagram

Core Features Overview

- Supports standard 4-Lane 100GBase-KR4 / CR4 / KP4 (IEEE 802.3bj), 100GBase-SR4 (IEEE 802.3bm) applications
- The Core can be used in proprietary 100Geth 2-Lane application with 50Gbps Serdes and PAM4 modulation
- Can be used together with any 100 Gigabit Ethernet PHY application or in integrated 100 Gigabit Ethernet controller devices
- Periodic Alignment Marker insertion / striping on transmit / receive, respectively
- Implements 100 Gigabit Ethernet data Scrambler on transmit and data De-Scrambler on receive
- 64b/66b Encoder / Decoder
- Programmable loopback on the Core CGMII interface available for application test
- Implements Bit Error Rate (BER) monitoring, with high error rate indication, providing constant line quality monitoring
- Programmable Reed-Solomon FEC supporting both RS(528,514) and RS(544, 514) compliant with the IEEE 802.3bj Clause 91 specification for use with NRZ and PMA4 modulations
- Transcodes four encoded and scrambled 66-bit blocks into compressed 257-bit units on transmit
- Decodes received 257-Bit units into four encoded and scrambled 66-Bit blocks on receive
- Synchronizes each serdes lane to the incoming marker patterns found to recover RS-FEC symbol and codeword boundaries

- Supports Correction Bypass for latency reduction
- Supports Error Indication to PCS when uncorrectable errors are detected
- Separate register access interface to allow merge with external PMA module registers
- Simple 16-Bit demultiplexed register interface
- Optionally includes standard 100Geth PCS MDIO Manageable Devices (MMD) register space
- Includes extended management and statistic registers

Implementation Summary

FEC Option	Memory (Bits)	Complexity (Gates)
With Error Propagation	49.808K	~520K

Ordering Code

MTIP-100G_KR4_PCS-lang-arch

Technology code

Language code

Language Code	*Delivery Language*
VLOG	Synthesizable RTL Verilog Source Code.

Technology Code	*Target Technology*
GEN	Generic synthesizable code for ASIC implementations

Contact

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