Single Lane 10/25/50 Gigabit Ethernet PCS Core

Product Brief Version 2.0 - April 2015

Introduction

The 10/25/50Gbps Ethernet PCS Core is compliant with the IEEE802.3 10/25Gbps and the 25G Ethernet Consortium 25Gbps Ethernet specifications allowing systems to support link speeds above 10Gbps, with no increase of the Trace and/or Cable interconnect density.

The Core can also be used with an embedded 50Gbps Serdes to implement single lane 50Geth interfaces.

The Core implements the standard IEEE 802.3 Clause 49 scrambler / descrambler and the 64b/66b encoder / decoder

The RS-FEC for 25Gbps and 50Gbps Serdes with NZR modulation uses RS(528, 514) codewords allowing correction of up to seven 10-Bit symbols within 514 symbols and the RS-FEC for 50Gbps Serdes with PAM4 modulation uses RS(544, 514) codewords allowing correction of up to 15 10-Bit symbols within 514 symbols.

With RS-FEC a MLD module distributes data across 4 virtual lanes. The 4 virtual lanes are then transcoded into RS-FEC codewords and transferred on the 25 / 50Gbps serial lane.

On receive, the MLD re-aligns the serial data stream to the RS-FEC codeword boundaries for allowing error correction and decode.

The Core optionally supports the IEEE Clause 74 Firecode FEC (FC-FEC) in addition to the IEEE Clause 91 Reed Solomon FEC (RS-FEC).

The RS-FEC and FC-FEC error propagation to the PCS can be bypassed with software programming or can be removed with a synthesis option to reduce the Core latency.

On the application side, the Core implements a 64-Bit XGMII (10 Gigabit Media Independent Interface).

On the line side, the Core implements a flexible 20, 40 or 64-bit parallel interface connectable to Industry standard embedded 10.3125Gbps, 25.78125Gbps and 51.5625Gbps Serdes macros.

The PCS Core can be used with MorethanIP Link Training and Autonegotiation Cores to design flexible backplane interconnection solutions.

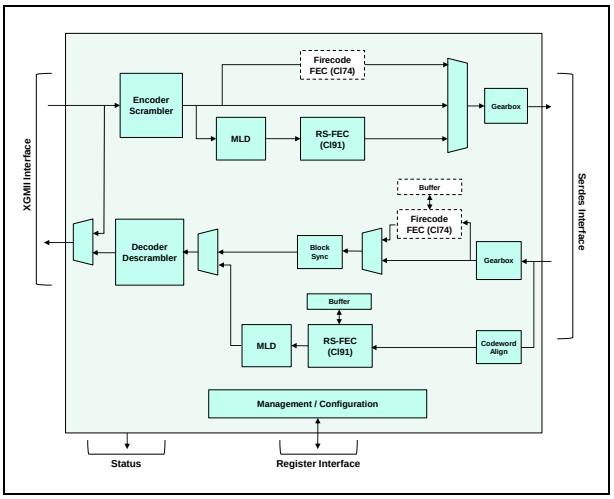
The Core is optimized for latency and can be used to design Synchronous Ethernet applications

The MorethanIP Clause 73 Autonegotiation Core is fully generic and supports 'Next Page' negotiations to select the, non IEEE, 25Geth and 50Geth modes of operation.

The Core is delivered in generic synthesizable technology independent Verilog HDL code.

The Core is delivered with a comprehensive verification environment and expert MorethanIP technical and application support.

Block Diagram



Core Block Diagram

Core Features

- Compliant with IEEE802.3 Clause 49 10Geth and 25G Ethernet Consortium 25Geth Specification Version 1.5
- The Core can be used in proprietary 50Geth single lane applications
- Optimized for Low latency and usable in Synchronous Ethernet applications
- For 25Geth and 50Geth operation implements a programmable Reed-Solomon FEC supporting both the RS-FEC(528, 514) and RS-FEC(544, 514) both compliant with the IEEE 802.3bj Clause 91 specification
- Dynamically configurable Serdes PMA interface width to optimize the Core latency for each mode of operation
- Multi-Lane Distribution (MLD) across 4 Virtual Lanes multiplexing over a single 25Gbps or 50Gbps Serdes lane with RS-FEC
- In MLD mode, the Core inserts periodic Alignment Marker insertion / striping on transmit / receive, respectively
- 64b/66b Encoder / Decoder and Scrambler/Descrambler performing 66-bit block synchronization, 64b/66b receive path decoding, 64b/66b transmit path encoding, and 66b/64b transmit path conversion for block overhead bits
- Implements Bit Error Rate (BER) monitoring, with high error rate indication, providing constant line quality monitoring
- Optional Firecode FEC (Clause 74) and Auto-Negotiation functions (Clause 73) for 10/25/50GBase-KR applications
- The PCS can be used in 25Geth and 50Geth applications with or without the RS-FEC, with and without the FC-FEC

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- Optional support for 10Geth Energy-Efficient Ethernet (EEE) compliant with the EEE, 802.3az specification
- Internal programmable XGMII loopback
- Can be seamlessly connected to the MorethanIP Low Latency 64-Bit 10/25/40/50Gbps Ethernet MAC
- Management Registers access through direct 16-bit host interface, or optionally Extended MDIO (Clause 45) serial Management Data interface.

Implementation Summary

FEC Option		Memory (Bits)	Complexity (Gates)
RS-FEC	Without Error Propagation	10.944K	~310K
	With Error Propagation	15.056K	~320K
RS-FEC and FC-FEC	Without Error Propagation	17.120K	~340K
	With Error Propagation	18.232K	~340K

Round-Trip Delay

The PCS round trip delay of the PCS is measured from the Core XGMII transmit interface to the Core receive XGMII interface with the Core PMA transmit interface connected to the Core PMA receive interface with 0 delay loopback connection.

Mode	PCS Round Trip Delay without FEC
10Geth	37ns
25Geth	18ns
50Geth	10ns

The RS-FEC and FC-FEC functions, when implemented, add to the PCS latency specified above a delay that is proportional to the Line Rate and the FEC Frame size.

The FEC delay is reduced when the Error Propagation to the PCS is disabled.

Mode	PCS Round Trip Delay with RS-FEC(528, 514)		PCS Round Trip Delay with FC-FEC	
	Without Error Propagation	With Error Propagation	Without Error Propagation	With Error Propagation
10Geth	NA	NA	310ns	525ns
25Geth	300ns	500ns	125ns	215ns
50Geth	155ns	255ns	70ns	110ns

Deliverables

- Verilog Synthesizable RTL HDL
- Behavioral Verilog testbenches and Verification test cases
- Verilog Simulation regression suite
- Synthesis script for Synopsys Design Compiler
- Timing constraints is Synopsys SDC format
- Direct support by MorethanIP engineers

Ordering Code

MTIP-25_50G-LL-PCS-lang-tech

technology code

language code

Language Code	*Delivery Language*
VLOG	Synthesizable RTL Verilog Source Code.

Technology Code	*Target Technology*
GEN	Generic synthesizable code for ASIC

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