10/16 Gigabit Fibre Channel FC-1 Core Product Brief

Version 3.0 - April 2013

Introduction

The Fibre Channel (FC) is logically a bi-directional point-to-point serial data channel, structured for high performance information transport. Physically, Fibre Channel is an interconnection of one or more point-to-point links. Each link end terminates in a Port.

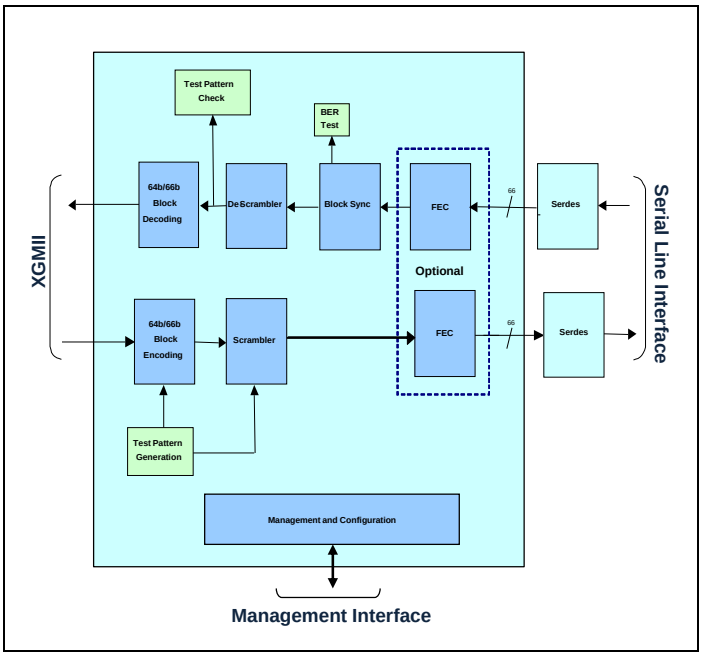
Ports are fully specified in the Physical Interface (FC-PI) specification and Framing and Signaling (FC-FS) specification. Fibre is a general term used to cover all physical media supported by Fibre Channel including optical fiber, twisted pair, and coaxial cable.

Fibre Channel is structured as a set of hierarchical functions and Fibre Channel consists of related functions FC-0 through FC-3. Each of these functions is described as a level. Fibre Channel does not restrict implementations to specific interfaces between these levels.

On the line side, the MorethanIP FC-1 Core, implements a 40-Bit interface, which can be connected to a Stratix IV GT or Stratix V embedded Serdes.

Optionally, the FC-1 Core can implement a Forward Error Correction (FEC). The FEC is compliant with the IEEE802.3ae Clause 74 and can be used to add margin to account for variations in manufacturing and environmental conditions.

The core is delivered in generic VHDL or Verilog synthesizable HDL code.



10/16G FC-1 Core Block Diagram

Core Features Overview

- Compliant with the IEEE802.3ae specification and UNH certified
- Compliant with the T11 10GFC, 16GFC and IEEE802.3ae specification
- 66-Bit Serdes interface
- Implements Serdes interface when the Core is implemented in an Altera Stratix V FPGAs
- Can implement a FEC(2112, 2080) Core compliant with the IEEE802.3ae Clause 74 specification.
- Implements data Scrambler which generates a transition rich signals to the application high speed optical link and data De-Scrambler on the Core receive path
- 64/66b data coder / decoder with synchronization bit insertion / deletion on transmit / receive respectively
- Supports reserved Clause 49 Reserved codes.
- 66b block synchronization on the receive path and 64b block encoding on transmit with gearbox function
- 64b/66b Encoder/Decoder performing 66-bit word alignment, the 64b/66b receive path decoding, the 64b/66b transmit path encoding, and the 66b/64b transmit path conversion for block overhead bits.
- Implements XGMII / XFI clock rates decoupling with elastic buffers on the transmit and receive paths
- Implements Test Pattern Generator/Checker for link testing implemented according to IEEE 802.3ae Clause 49.2.8 and 49.2.12.
- Implement Bit Error Rate (BER) monitoring, with high error rate indication, providing constant line quality monitoring
- Available on Altera Stratix FPGA devices and generics standard cell ASIC technologies

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Implementation Summary

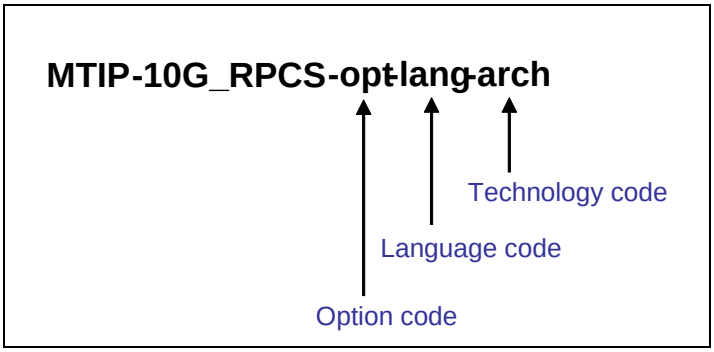
Altera FPGA Implementation Summary

Complexity with FEC			Performance Requirement
ALMs	**Registers**	**Memory Blocks**	
3300	4660	2 M20Ks (2080 Bits)	212.5MHz
Without FEC			
1950	1950	0	

Deliverables

- Verilog Synthesizable RTL HDL or encrypted RTL for FPGA implementation
- Behavioral Verilog testbenches and Verification test cases
- Support for Altera Quartus II FPGA design tools
- Support for industry standard ASIC design tools

Ordering Code



Option Code	*Option*
FEC	FEC functions.

Language Code	*Delivery Language*
VHDL	Synthesizable RTL VHDL Source Code.
VLOG	Synthesizable RTL Verilog Source Code.
BIN	Encrypted RTL for Altera FPGA technology.

Technology Code	*Target Technology*
GEN	Generic sythesizable code for ASIC or FPGA implementations
ALTR	Synthesizable code optimized Altera FPGAs.

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