16 Gigabit Fibre Channel FC-2 Core Product Brief

Version 1.0 – April 2013

Introduction

The Fibre Channel (FC) is logically a bi-directional point-to-point serial data channel, structured for high performance information transport. Physically, Fibre Channel is an interconnection of one or more point-to-point links.

Each link end terminates in a Port. Ports are fully specified in the Physical Interface (FC-PI) specification and Framing and Signaling (FC-FS) specification.

Fibre is a general term used to cover all physical media supported by Fibre Channel including optical fiber, twisted pair, and coaxial cable.

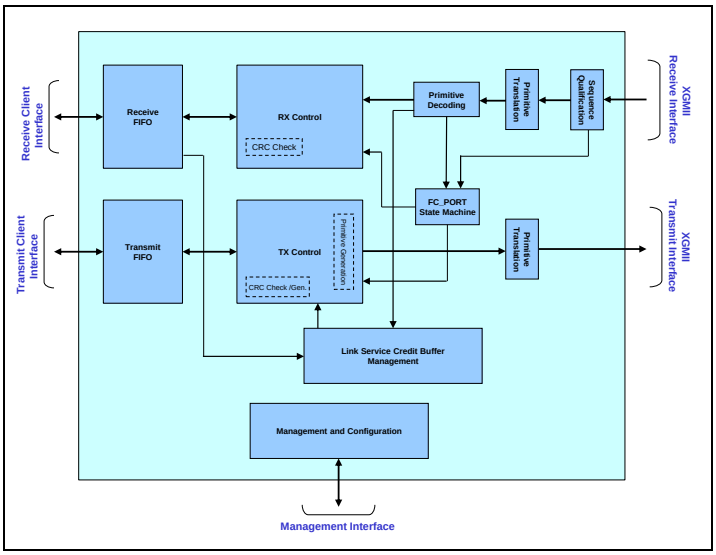
The 16 FC-2 Transport Core provides a generic solution for 14.025Gbps (16GFC) Fibre Channel applications. The core is designed to support standard Fibre Channel applications such as point-to-point and fabric interconnect.

On the Client side, the Core implements a 64-Bit FIFO interface running asynchronously from the Fibre Channel line clock.

The FC-2 Layer provides services such as CRC generation / check, generate Fibre Compliant frames and maintains buffer-to-buffer credit and necessary Fibre Channel timers.

The core is designed to support standard Fibre Channel applications such as point-to-point and fabric interconnect and can be used in conjunction with MorethanIP Ethernet Cores in FcoE (Fibre Channel over Ethernet) applications.

The core is delivered in generic source or encrypted Verilog synthesizable HDL code.



16 Gigabit FC-2 Transport Core Block Diagram

16GFC Fibre Channel Transport Core Features

- Support s 16GFC applications
- Seamless interface MorethanIP 16GFC-1 PCS Core
- Built-In client interface FIFO providing rate and clock decoupling
- Implement Fibre Channel primitive generation and decoding
- Fibre Channel Sequence qualification State Machine
- Maintains Fibre Channel IDLE primitive stream between frame transmission and ensures that frames are separated by a minimum of 24-Bytes.
- Simple 64-Bit FIFO interface to user client application compatible with Altera Atlantic specification
- CRC-32 checking at wire speed using a multi-stage CRC calculation architecture
- Optional CRC check and correction on the Core transmit path controllable on a frame by frame basis
- Frame minimum and maximum length verification with long frame truncation and error indication
- Implements Fibre Channel FC_PORT Port control state machine with programmable timers
- Core configurable as N_Port with automatic discard of Class F traffic or as F_Port capable of processing class F traffic
- Provide FC Transport support for point-to-point Fibre Channel applications
- Support any Fibre Channel Traffic Class and Frame termination condition
- Implement Buffer-to-Buffer Credit management with Credit recovery, credit reset and automatic R_RDY, BB_SCr and BB_SCs primitives generation
- Programmable 16-Bit credit recovery timer
- Programmable Transmit and Receive FIFO depth
- Simple handshake user application FIFO interface with full rate back-to-back frame transfer ability
- Available on Altera Stratix FPGA devices and generics standard cell ASIC technologies

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Implementation Summary

Altera Implementation Summary

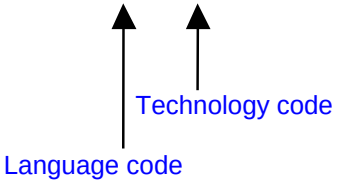
Complexity			Performance Requirement
ALMs	**Registers**	**Memory Bits** (32x64 FIFOs)	
3250	2560	5096	212.5MHz

Deliverables

- Verilog Synthesizable RTL HDL or encrypted RTL for FPGA implementation
- Behavioral Verilog testbenches and Verification test cases
- Support for industry standard ASIC design tools

Ordering Code

MTIP-10_16G_FC_2-lang-arch



Language Code	*Delivery Language*
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VHDL	Synthesizable RTL VHDL Source Code.
VLOG	Synthesizable RTL Verilog Source Code.
BIN	Encrypted RTL for Altera FPGA technology.

Technology Code	*Target Technology*
GEN	Generic sythesizable code for ASIC or FPGA implementations
ALTR	Synthesizable code optimized Altera FPGAs.

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