# 1/2/4/8Gbps Fibre Channel Transport Core

Version 1.0 - April 2009

## *Introduction*

The Fibre Channel (FC) is logically a bi-directional point-to-point serial data channel, structured for high performance information transport. Physically, Fibre Channel is an interconnection of one or more point-to-point links.

Each link end terminates in a Port. Ports are fully specified in the Physical Interface (FC-PI) specification and Framing and Signaling (FC-FS) specification.

Fibre Channel is a general term used to cover all physical media supported by Fibre Channel including optical fiber, twisted pair, and coaxial cable.

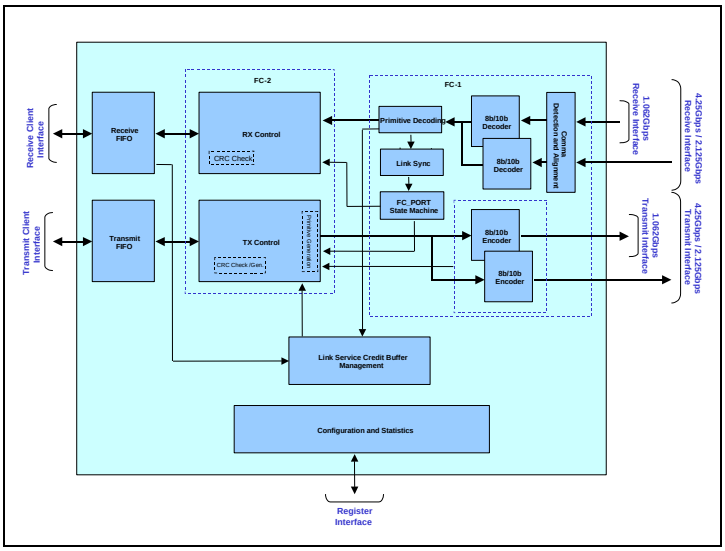
The 1/2/4Gbps FC-2 Transport Core provides a generic solution for 1Gbps to 4Gbps Fibre Channel applications. The core is designed to support standard Fibre Channel applications such as point-to-point and fabric interconnect.

On the Client side, the Core implements a 16-Bit or 32-Bit FIFO interface running asynchronously from the Fibre Channel line clock.

The FC-2 Layer provides services such as CRC generation / check, generate Fibre Compliant frames and maintains buffer-to-buffer credit and necessary Fibre Channel timers.

The core is designed to support standard Fibre Channel applications such as point-to-point and fabric interconnect and can be used in conjunction with MorethanIP Ethernet Cores in FcoE (Fibre Channel over Ethernet) applications.

The core is delivered in generic source or encrypted Verilog synthesizable HDL code.




**1/2/4Gbps Fibre Channel Transport Core Block Diagram**

## *1/2/4Gbps Fibre Channel Transport Core Features*

- Configurable to support Gigabit (106.25Gbps Baud Rate), 2 Gigabit (2.12Gbps Baud rate) or 4 Gigabit (4.24Gbps Baud rate) Fibre Channel applications
- Seamless interface to commercial or embedded SERDES via a standard 40-Bit interface
- Simple 6-Bit or 32-Bit FIFO interface to user client application
- CRC-32 checking at wire speed using a multi-stage CRC calculation architecture
- Frame minimum and maximum length verification with long frame truncation and error indication
- Programmable maximum frame length to any value up to 4096 Bytes with default length set to 2136 bytes
- Link coding implemented with 8b/10b providing DC balanced bitstream for efficient SERDES operation
- Maintain 8b/10b current disparity rules with automatic correction using positive or negative encoded EOF primitives
- Implements FC-1 link synchronization with Loss of Synchronization indication
- Implements Fibre Channel FC_PORT Port control state machine with programmable timers
- Core configurable as N or F Fibre Channel port with automatic Fabric frames discard (N Port configuration)
- Provide FC Transport support for point-to-point Fibre, fabric Fibre Channel applications
- Support any Fibre Channel Traffic Class and Frame termination condition
- Implement Buffer-to-Buffer Credit management with credit recovery, credit reset and automatic R_RDY, BB_SCr and BB_SCs primitives generation
- Programmable 16-Bit credit recovery timer
- Programmable Transmit and Receive FIFO depth
- Implements processor control interface with 32-Bit statistic counters and configuration registers
- Available on Altera Stratix, Arria and Cyclone FPGA devices, Xilinx Spartan, Kintex and Virtex FPGA devices and generics standard cell ASIC technologies

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## *Implementation Summary*

**Altera FPGA Implementation Summary**

| Complexity | | | Performance Requirement |
|---|---|---|---|
| **ALUTs** | **Registers** | **Memory Bits** (128x16 FIFOs) | |
| 2110 | 2490 | 7173 | 4GFC: 212.5MHz<br>3GFC: 106.25MHz<br>1GFC: 53.125MHz |

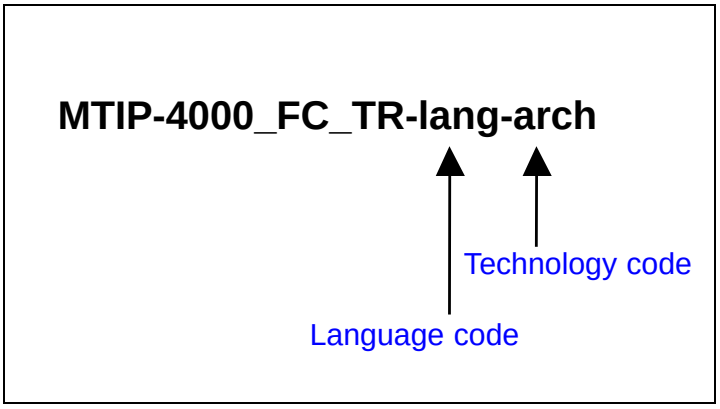
**Xilinx FPGA Implementation Summary**

| Complexity | | | Performance Requirement |
|---|---|---|---|
| **Slices** | **Registers** | **Memory Bits** (128x16 FIFOs) | |
| 1270 | 2490 | 7173 | 4GFC: 212.5MHz<br>3GFC: 106.25MHz<br>1GFC: 53.125MHz |

## *Deliverables*

- Verilog Synthesizable RTL HDL or encrypted RTL for FPGA implementation
- Behavioral Verilog testbenches and Verification test cases
- Support for Altera Quartus II or Xilinx ISE FPGA design tools
- Support for industry standard ASIC design tools

## *Ordering Code*




| *Language Code* | *Delivery Language* |
|---|---|
| VHDL | Synthesizable RTL VHDL Source Code. |
| VLOG | Synthesizable RTL Verilog Source Code. |
| BIN | Encrypted RTL for Altera FPGA technology. |

| *Technology Code* | *Target Technology* |
|---|---|
| GEN | Generic sythesizable code for ASIC or FPGA implementations |
| ALTR | Synthesizable code optimized Altera FPGAs. |
| XLX | Synthesizable code optimized Xilinx FPGAs. |

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