32 Gigabit Fibre Channel FC-1 Core Product Brief

Product Brief
Version 1.0 - January 2014

Introduction

The Fibre Channel (FC) is logically a bi-directional point-to-point serial data channel, structured for high performance information transport. Physically, Fibre Channel is an interconnection of one or more point-to-point links.

Each link end terminates in a Port. Ports are fully specified in the Physical Interface (FC-PI) specification and Framing and Signaling (FC-FS) specification.

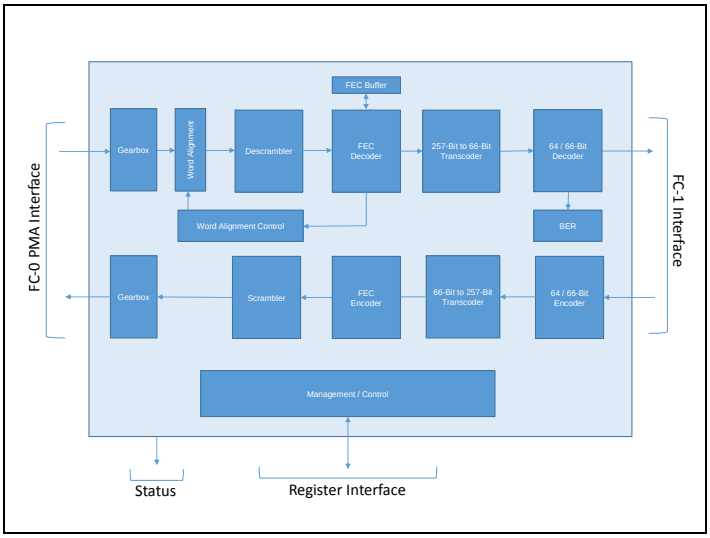
Fibre is a general term used to cover all physical media supported by Fibre Channel including optical fiber, twisted pair, and coaxial cable.

The 32 FC-1 Core provides a generic solution for 28.050Gbps (32GFC) Fibre Channel applications. The core is designed to support standard Fibre Channel applications such as point-to-point and fabric interconnect.

On the System side, the Core implements a 64-Bit XGMII interface and can be connected 32GFC-2 Layer provides services such as CRC generation / check, generate Fibre Compliant frames and maintains buffer-to-buffer credit and necessary Fibre Channel timers.

The core is delivered in generic source Verilog synthesizable HDL code.

Block Diagram



32 Gigabit FC-1 Transport Core Block Diagram

32GFC-1 Fibre Channel Core Features

- Compliant with T11 FC-FS-4 standard
- 64-Bit FC-1 interface to MorethanIP 32 Gigabit FC-2 Transport Core or third party logic
- 64/66b data coder / decoder with synchronization header insertion / deletion on transmit / receive respectively
- Encoder and Decoder supports all Ethernet and Fibre Channel XGMII sequence types
- Can operate at different rates on Receive and Transmit independently
- Data compression with 257-Bit block transcoding (Tx) and inverse transcoding (Rx)
- Implements Reed-Solomon Forward Error Correction (RS-FEC):
  - IEEE802.3bj Clause 91 RS-FEC using RS(528, 514) codewords
  - Can correct up to 7 bit error is every RS-FEC block (RS-FEC codeword)
  - Implements programmable error injection on the Transmit path
  - Supports for Correction Bypass for latency reduction
  - Supports for Error Indication to PCS when uncorrectable errors are detected
- RS-FEC codeword scrambling and descrambling
- Automatic word alignment
- Test pattern generation and checking controlled with registers
- Programmable loopback on the Core FC-1 interface available for application test
- Implement Bit Error Rate (BER) monitoring, with high error rate indication, providing constant line quality monitoring
- FC-0 Serdes interface width programmable with a synthesis parameter to 64, 40 or 32 Bits
- Management and configuration with a 16-Bit parallel Register interface
- Available generics standard cell ASIC technologies

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Implementation Summary

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Resources Used	
Gates	~430,000
Memory Bits	19,472
Provided with the Core	
Documentation	Datasheet, User Guide
Design File Formats	Source RTL Verilog
Constraints File	SDC File
Verification	Verilog Self-Checking Testbench Verilog Regression Suite
Supported Design Tools	
Simulation	Mentor Modelsim, Synopsys VCS Verilog Simulation Tools
Synthesis	Synopsys Design Compiler Verilog Synthesis Tools

Language Code	*Delivery Language*
VLOG	Synthesizable RTL Verilog Source Code.

Technology Code	*Target Technology*
GEN	Generic sythesizable code for ASIC implementations

Deliverables

- Verilog Synthesizable RTL HDL
- Behavioral Verilog testbenches and Verification test cases
- Support for industry standard ASIC design tools

Ordering Code

MTIP-32_GFC_1-lang-arch

Technology code

Language code

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